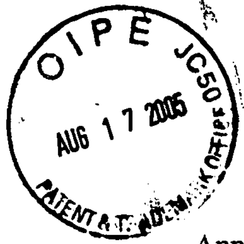

Express Mail No. EV530953239US

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	:	Osama Khouri et al.
Application No.	:	10/756,195
Filed	:	January 13, 2004
For	:	SUBLITHOGRAPHIC CONTACT STRUCTURE, IN PARTICULAR FOR A PHASE CHANGE MEMORY CELL, AND FABRICATION PROCESS THEREOF

Examiner	:	Thanhha S. Pham
Art Unit	:	2813
Docket No.	:	854163.412

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

BEST AVAILABLE COPY

DECLARATION

Commissioner for Patents:

I, Elena Cerbaro, residing at Corso Raffaello 15 Torino, Italy, declare as follows:

I am a European Patent Attorney who prepared and filed on January 15, 2003 European Patent Application 03425016.7, from which the application identified above claims priority.

Attached as Appendix 1 is a printed copy of an email sent to me by Fabio Pellizzer, who is one of the co-inventors of the present application, dated prior to December 13, 2002 (see English translation included in Appendix 1). The email included an attached draft patent application which describes in detail the claimed invention.

Attached as appendix 2 is a printed copy of an email received by me from Fabio Pellizzer, dated prior to December 13, 2002 (see English translation included in Appendix 2). Shown at the bottom of the printed copy in Appendix 2 is a first handwritten note that I wrote indicating that I had a telephone conference on December 13, 2002 with Roberta Radaelli, who is a patent attorney in the patent department of STMicroelectronics, Srl, which is one of the

assignees of the present application. The first handwritten note indicates that Roberta Radaelli told me that we were waiting for an approval of the draft patent application from Ovonyx, which is another one of the assignees of the present application.

Also shown at the bottom of the printed copy in Appendix 2 is a second handwritten note that I wrote indicating that I had another telephone conference on January 8, 2003 with Roberta Radaelli. The second handwritten note indicates that Roberta Radaelli told me that the text had already been reviewed by Ovonyx and that they had made small amendments. The second handwritten note also indicates that Roberta Radaelli told me that the draft was being reviewed by Roberto Bez, who was the person in charge of the technical aspects of phase change memories at STMicroelectronics.

I believe that the inventors, assignees, and I took diligent steps to prepare and file European Patent Application 03425016.7 during the period beginning just prior to December 13, 2002 and ending with the January 15, 2003 filing of European Patent Application 03425016.7. My belief is supported by the handwritten notes on the printed copy of the email in Appendix 2 and by the fact that the European application was filed only approximately one month after December 13, 2002. In my experience, such a relatively short period indicates that diligent steps were taken to file the European application, especially in view of the fact that the European application was being filed pursuant to a joint venture by STMicroelectronics Srl, an Italian company, and Ovonyx, an American company.

In summary, I believe that the claimed invention of the present application was conceived by the inventors prior to December 13, 2002, and the invention was diligently reduced to practice by completing preparation and review of a draft patent application and then filing the European Patent Application No. 03425016.7 on January 15, 2003.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

July 28, 2005
Date

Elena Cerbaro

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615332_1.DOC

Express Mail No. EV530953239US
Appendix 1

Elena Cerbaro

Da: "Fabio Pellizzer" <fabio.pellizzer@st.com>
A: "Elena Cerbaro" <cerbaro@studiotorta.it>
Cc: <roberto.bez@st.com>; <giorgio.pollaccia@st.com>; "Roberta Radaelli (ST)" <roberta.radaelli@st.com>; "Osama Khouri" <Osama.KHOURI@st.com>
Data invio:
Allega: 02-AG-300.zip
Oggetto: Re: Fw: 02-AG-300/RR

Buongiorno Ing. Cerbaro.

Chiedo scusa per il colpevole ritardo.

In allegato trova il file .zip con le correzioni (solita password).

Mi faccia sapere se ci sono problemi.

Fabio

cerbaro@studiotorta.it wrote:

\> ____ Ricordo che non ho ancora
\> avuto vostre indicazioni e commenti sul testo inviato. Elena Cerbaro
\> Studio Torta
\> Tel: 0039/011/561.13.20
\> ________________
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From: Fabio Pellizzer <fabio.pellizzer@st.com>
To: Elena Cerbaro
Cc: roberto.bez@st.com; giorgio.pollaccia@st.com; Roberta Radaelli (ST); Osama Khouri
Sent:
Attached: 02-AG-300-1.2.zip
Subject: Re: Fw: 02-AG-300/RR

Good morning Ing. Cerbaro,

Please excuse my delay.

Attached is the .zip file with the corrections (usual password).

Let me know if there are problems.

Fabio

cerbaro@studiotorta.it wrote:

> ____ I remind you that I do not yet have your
> information and comments on the text that I sent. Elena Cerbaro
> Studio Torta
> Tel: 0039/011/561.13.20 ____________________
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SUBLITHOGRAPHIC CONTACT STRUCTURE, IN PARTICULAR FOR A PHASE CHANGE MEMORY CELL, AND FABRICATION PROCESS THEREOF

(02-AG-300/RR)

5 Inventors: KHOURI Osama, POLLACCIA Giorgio, PELLIZZER Fabio

The present invention relates to a sublithographic contact structure, in particular for a phase change
10 memory cell, and a fabrication process thereof.

As is known, phase change memory cells utilize a class of materials that have the unique property of being reversibly switcheable from one phase to another with measurable distinct electrical properties
15 associated with each phase. For example, these materials may change between an amorphous disordered phase and a crystalline, or polycrystalline, ordered phase. A material property that may change and provide a signature for each phase is the material resistivity,
20 which is considerably different in the two states.

At present, alloys of elements of group VI of the periodic table, such as Te or Se, referred to as chalcogenides or chalcogenic materials, can advantageously be used in phase change cells. The
25 currently most promising chalcogenide is formed by a

Ge, Sb and Te alloy ($Ge_2Sb_2Te_5$), which is currently widely used for storing information in overwritable disks.

In chalcogenides, the resistivity varies by two or
5 more magnitude orders when the material passes from the amorphous phase (more resistive) to the polycrystalline phase (more conductive) and vice versa, as shown in Figure 1. Furthermore, in the amorphous phase, resistivity strongly depends also on temperature, with
10 variations of one magnitude order every 100°C, with a behavior similar to that of P-type semiconductor materials.

Phase change may be obtained by locally increasing the temperature, as shown in Figure 2. Below 150°C both
15 phases are stable. Above 200°C (temperature of start of nucleation, designated by T_x), fast nucleation of the crystallites takes place, and, if the material is kept at the crystallization temperature for a sufficient time (time t_2), it changes its phase and becomes
20 crystalline. To bring the chalcogenide back into the amorphous state, it is necessary to raise the temperature above the melting temperature T_m (approximately 600°C) and then to cool the chalcogenide off rapidly (time t_1).

25 From the electrical standpoint, it is possible to

reach both critical temperatures, namely the crystallization and the melting temperatures, by causing a current to flow through a crystalline resistive element which heats the chalcogenic material
5 by the Joule effect.

The basic structure of a PCM element 1 which operates according to the principles described above is shown in Figure 3 and comprises a first electrode 2 (of resistive type, forming a heater); a programmable
10 element 3 and a second electrode 5. The programmable element 3 is made of a chalcogenide and is normally in the polycrystalline state in order to enable a good flow of current. One part of the programmable element 3 is in direct contact with the first electrode 2 and
15 forms the active portion affected by phase change, hereinafter referred to as the phase change portion 4.

In the PCM element 1 of figure 3, technological and electrical considerations impose that the contact area between the first electrode and the programmable
20 element has small dimensions, so that, for the same current density, the writing operation may be carried out at the required thermal energy with smaller current consumption.

Several proposal have been done for reducing the
25 contact area. For example, US-A-6,294,452 discloses a

process for forming a contact area of sublithographic dimensions, based on isotropically etching a polysilicon layer. The resulting sublithographic dimensions depend on the quality of the etching.

5 US 2001/0002046 discloses a process for forming an electrode of a chalcogenide switching device, wherein a spacer layer deposited in a lithographic opening is anisotropically etched and laterally defines an electrode. The resulting width of the electrode depends

10 on the thickness of a spacer layer.

Patent application 01128461.9, filed on 5.12.2001, and entitled "Small area contact region, high efficiency phase change memory cell, and manufacturing method thereof", teaches forming the contact area as an

15 intersection of two thin portions extending transversely with respect to one another and each of a sublithographic size. In order to form the thin portions, deposition of layers is adopted.

In all the indicates prior solutions, any

20 variation in the electrode width L (Figure 3), due for example to the process tolerances, affects, in a linear way, the contact area of the active region 4. Thus, the width L may have tolerances that are not acceptable as regards repeatability and uniformity of the cell

25 characteristics.

The object of the invention is thus to provide a contact region having an area less dependent on the process variations.

According to the present invention, there are provided a electronic semiconductor device and a process for manufacturing an electronic semiconductor device, as defined respectively in claims 1, and 9.

According to one aspect of the invention, the contact area is formed laterally to the active region and has a height and width. Advantageously, the height of the contact area is determined by the thickness of a deposited layer, which is technologically controlled and may be designed to be sublithografic. Furthermore, according to another aspect of the invention, the width of the contact area is determined by the width of a spacer which may also be designed of sublithographic dimensions and may be dimensionally controlled with a good accuracy.

For the understanding of the present invention, a preferred embodiment is now described, purely as a non-limitative example, with reference to the enclosed drawings, wherein:

- Figure 1 illustrates the characteristic current-voltage of a phase change material;

- Figure 2 shows the temperature versus current

plot of a phase change material;

- Figure 3 shows the basic structure of a PCM memory element;

- Figure 4 shows a cross section of a contact
5 structure according to the present invention;

- Figure 5 is a perspective view of a portion of the contact structure of Figure 4 showing the variability of the contact area due to technological tolerances;

10 - Figure 6 is a cross-section of a PCM memory element in an initial manufacturing step;

- Figures 7-11 are cross-sections of an enlarged detail of Figure 6, in subsequent manufacturing steps;

- Figure 12 is a perspective view of the structure
15 of Figure 11; and

- Figures 13-16 are cross-sections of the PCM memory element, in subsequent manufacturing steps, taken in a perpendicular plane with respect to Figures 7-11.

20 Figure 4 illustrates the basic structure of a contact structure according to the invention. In detail, an electronic device 90 has a body 91 (e.g. a substrate) of monocrystalline material defining an upper surface 92 and a lower surface 93 and
25 accommodating electronic components 94, represented

schematically. A dielectric layer 95 extends on top of the body 91 and accommodates the contact structure, indicated at 98. The contact structure 98 is formed by a first electrode 100 and an active region 103 of
5 chalcogenic material. The first electrode 100, connected to the electronic components 94 as shown schematically for one of them, has a horizontal portion 102 adjacent to and in contact with the active region 103. A second electrode 104 is formed on the active
10 region 103 and is in electric contact therewith.

As better shown in the perspective view Figure 5, the horizontal portion 102 has an elongated shape extending along a longitudinal direction X parallel to the upper and lower surfaces 92, 93 of the body 91. The
15 horizontal portion 102 is longitudinally delimited by an end face 110. The end face 110 extends in a vertical plane, which is ideally perpendicular to the longitudinal direction X and thus to the upper and lower surfaces 92, 94 and defines a lateral contact
20 area with the active region 104. The end face 110 is here rectangular and has a height S (extending parallel to direction Z) and a width W (extending parallel to direction Y). The portion of the active region 104 adjacent to the end face 110 undergoes phase change and
25 thus corresponds to the active region 4 of Figure 3.

Because of the vertical arrangement of the end face 110 and thus of the contact area, the height S is equal to the thickness of the horizontal portion 102 of the first electrode 100, and thus may be designed to be
5 sublithographic, that is smaller than the minimum dimension obtainable through optical UV lithography.

In practice, the contact structure 98 according to Figures 4, 5 is formed by an elongated formation (horizontal portion 102 of the first electrode 100)
10 having a longitudinal extension parallel to the upper surface 92 of the body 91 and an end face 110 extending in a vertical plane and in contact with the active region 103 so that the dimensions of the contact area (defined by the end face 110) are determined by the
15 thickness S of the elongated formation and by the width W thereof.

The height S of the horizontal portion 102 and thus of the contact area is more controllable than the electrode width L of prior art contact structures
20 (Figure 3), so that PCM cells having the contact structure of Figure 4 have more uniform dimensions than prior art cells. The thickness tolerance of a conductive layer forming the horizontal portion 102 allows, for same overall dimensions, a higher
25 constructive confidence than electrodes the contact

area whereof depends on the width L.

The height S also depends on the quality of the operation used to define the end face 110, in particular by the etching operation used to this end.
5 Figure 5 shows the possible variation of the contact area in case etching does not ensure exact verticality of the end face 110, so that horizontal portion 102 has an inclined end face, indicated at 110', forming an angle α with ideal end face 110 (which, as said, is
10 perpendicular to the upper surface 92). In this case, the height S' of the inclined end face 110' is greater than height S by a quantity depending on the angle α, since

$$S' = S/\cos\alpha.$$

15 In the worst cases, with current technologies, $\alpha \leq 5°$, so that $\cos\alpha \cong 1$ [$\cos(5°)=0.99619$]. Since any variation of height S has the same impact on the contact area, the variation of the contact area due to process tolerances affecting the height S is lower than
20 2%.

Furthermore, also the width W may be sublithographic, by exploiting the spacer technique, as discussed later on, with reference to Figures 7-12. This technique has a tolerance of ±10%.

25 The process for manufacturing the contact structure

of Figure 4 will be now described, with reference to Figures 6-16.

First, Figure 6, a wafer 10 comprising a P-type substrate 11 having an upper surface 16 is subjected to
5 standard front end steps. In particular, inside the substrate 11 insulation regions 12 are formed and delimit active areas; then, in succession, base regions 13 of N-type, base contact regions 14 of N^+-type, and emitter regions 15 of P^+-type are implanted. The base
10 regions 13, base contact regions 14, and emitter regions 15 form diodes or bipolar transistors that define selection elements for the memory cells.

Next, a first dielectric layer 18 is deposited and planarized; openings are formed in the first dielectric
15 layer 18 above the base contact regions 14 and emitter regions 15, and the openings are filled with tungsten to form emitter contacts 19a and base contacts 19b. Then, a second dielectric layer 20 -for example, an undoped silicon glass (USG)- is deposited, and openings
20 21, for example, cylindrical-shaped, are formed in the second dielectric layer 20 above the emitter contact 19a. Next, a cup-shaped region 22 is formed, e.g. by depositing an electrode layer, for example of TiSiN, TiAlN or TiSiC, that conformally coats the walls and
25 bottom of the openings 21 and is subsequently removed

outside the openings 21. The cup-shaped region 22 thus has a vertical wall 22a extending along the cylindrical side surface of the openings 21. The remaining portions of the electrode layer are then filled with dielectric material 23.

Then, a first conductive layer 27 (for instance TaSiN, TiSiN, TiN, TiAlN, etc.) having a thickness of 5-50 nm, corresponding to the desired height S of the contact area 110, thus obtaining the structure of Figure 6. As visible, the first conductive layer 27 extends parallel to the upper surface 16 of substrate 11.

At this point, a mask is exposed and the conductive layer 27 is selectively etched in order to form stripes parallel to the y-direction.

The width of these stripes has to be enough to touch the conductive ring on one side and to be cut by the trench etch described in Fig.14 on the other side.

Next, Figure 7, a delimiting layer 29 of insulating material, for example **oxide**, is deposited. The delimiting layer 29 has a thickness of, for instance, 20-200 nm. Then, using a mask, one part of the delimiting layer 29 is removed by dry etching to form a step which has a vertical side 30 that extends vertically on top of the dielectric material 23, and

crosses the vertical wall 22a of cup-shaped region 22 (at a point located before or behind the drawing plane, and thus not visible in Figure 7).

Next, a sacrificial layer 31, for example nitride
5 with a thickness of 5-50 nm, is deposited conformally. In particular, the sacrificial layer forms a vertical wall 31a that extends along the vertical side 30 of the delimiting layer 29. Thus, the structure of Figure 7 is obtained.

10 Thereafter (Figure 8), the sacrificial layer 31 undergoes an anisotropic etching that results in removal of the horizontal portions of the sacrificial layer 31 and of part of the vertical wall 31a. By appropriately choosing the thickness of the delimiting
15 layer 29 and the thickness of the sacrificial layer 31, as well as the time and type of etching, it is possible to obtain the desired sublithographic width W for the bottom part of the remaining vertical wall 31a.

Then, Figure 9, the remaining portion of the
20 delimiting layer 29 is removed and, Figure 10, using the vertical wall 31a as a hard mask, the first conductive layer 27 is defined. Thereafter, Figure 11, the vertical wall 31a is removed.

Now, as shown in perspective in Figure 12, the
25 remaining portion of the first conductive layer 27

(strip-shaped portion 27a) has a height S and a width W.

Thereafter, Figure 13, an insulating layer 30 (e.g. silicon oxide) and a second adhesion layer 31 (e.g. Si,
5 Ti, Ta, etc.) are deposited in sequence.

Then, Figure 14, a trench 32 of lithographic dimensions is opened. The trench 32 is an aperture having a preset length in the direction perpendicular to the drawing sheet and intersects the strip-shaped
10 portion 27a and extends within the second dielectric layer 20 so as to longitudinally delimit the strip-shaped portion 27a. In practice, the trench 32 determines the length L1 of the strip-shaped portion 27a.

15 Thereafter, Figure 15, a chalcogenic layer 33, for example of $Ge_2Sb_2Te_5$ having a thickness of e.g. ???, is conformally deposited and fills the trench 32 with a reduced area portion 33b the shape and dimensions whereof are determined by the trench 32.

20 Then, a barrier layer 34, for example of Ti/TiN, and a metal layer 35, for example of AlCu, are deposited in sequence on top of the chalcogenic layer 33; the stack formed by the metal layer 35, the barrier layer 34 and the chalcogenic layer 33 is defined using
25 a same mask, thus forming a bit line 41 including a

chalcogenic region 33a and metal regions 34a, 35a. Finally, a third dielectric layer 42 is deposited, which is opened above the base contacts 19b. The openings thus formed are filled with tungsten to form
5 top contacts 43 in order to prolong upwards the base contacts 19b. Then standard steps are performed for forming connection lines in contact with the top contacts 43 and with the bits lines 41, pads are formed and a passivation layer 45 is deposited, defining a
10 device main surface 46. Thus, the final structure of Figure 16 is obtained.

In practice, the strip-shaped portion 27a (corresponding to the horizontal portion 102 of the first electrode 100 of Figure 4) has a longitudinal
15 extension parallel to upper surface 16 of the substrate 11 and forms, with the bottom portion of the reduced area portion 33b, a contact area the height whereof is defined by the thickness of the first conductive layer 27 and the width whereof is defined by the thickness of
20 the sacrificial layer 31. The quality of the etching of trench 32 determines the orientation of the contact area with respect to the upper surface 16.

The advantages of the present invention are clear from the above. In particular, it is outlined that the
25 present contact structure has a very good technological

repeatability, a lower dependence from the process variations than prior art solutions, while maintaining a very small contact area, having sublithographic dimensions in both directions.

5 Finally, it is clear that numerous variations and modifications may be made to the contact structure and process described and illustrated herein, all falling within the scope of the invention as defined in the attached claims.

10 In particular, it is stressed that the direction of the horizontal portion 102 and the first conductive layer 27 is defined with reference to the upper surface 92, 16 of the substrate, intending therewith a plane corresponding to the original upper surface of the
15 wafer. In practice, the horizontal portion 102 and the first conductive layer 27 are perpendicular to the direction of growing of the substrate, due to the deposition of the various superficial layers. If, due to deposition, thermal growing, etching and implant
20 steps carried out on the wafer, the upper surface 16 of the finished device is no more planar, reference may be done to the lower surface 93 of the substrate or to the device main surface 46.

Moreover we propose an alternative embodiment of
25 the present invention in which the conductive layer 27

is in direct contact with the conductive layer 19a, thus avoiding the dielectric layers 20 and 23 and the conductive layer 22.

CLAIMS

1. An electronic semiconductor device (90), comprising:

a body (91; 11) of semiconductor material having an upper surface (92; 16);

a dielectric layer (95; 20, 42) extending on top of said body;

a contact structure (98) in said dielectric layer, said contact structure comprising a first conducting region (102; 27a) and a second conducting region (103; 33a), said second conducting region being of chalcogenic material and being in electric contact with said first conducting region;

characterized in that said first conducting region (102; 27a) has a strip-like shape having a longitudinal direction delimited by an end face (110) extending transversely to said upper surface (92; 16) and forming a contact area with said second conducting region (103; 33a).

2. A device according to claim 1, wherein said first conducting region (102; 27a) extends in a first direction (X) parallel to said upper surface (92; 16).

3. A device according to claim 1 or 2, wherein said end face (110) is perpendicular to said upper surface

(92; 16) within process tolerances.

4. A device according to any of claims 1-3, wherein said end face (110) has a generally rectangular shape having a height (S) and a width (W).

5 5. A device according to claim 4, wherein said height (S) is comprised between 5 nm and 50 nm and said width (W) is comprised between 5 nm and 50 nm.

6. A device according to any of claims 1-4, forming a PCM device (10) including a memory cell comprising a 10 selection element (13-15) and a storage element, said storage element being formed by a heater element (22a, 27a) including said first conducting region (27a) and a storage region (33a) comprising said second conducting region.

15 7. A device according to claim 6, wherein said selection element (13-15) is formed in said body (11), a lower electrode (19a) extends in said dielectric layer (20, 42) between said selection element and said first conducting region (27a) and an upper electrode 20 (35a) extends in said dielectric layer on said second conducting region (33a) and forms a bit line.

8. A device according to claim 7, wherein said second conducting region (33a) has a reduced area portion (33b) in contact with said first conducting

region (27a) and an upper enlarged portion extending on top of said reduced area portion and in contact with said upper electrode (35a).

9. A process for manufacturing an electronic
5 semiconductor device (10), comprising the steps of:

providing a body (91; 11) of semiconductor material having an upper surface (92; 16);

forming a dielectric layer (95; 20, 42) extending on top of said body; and

10 forming a contact structure (98) in said dielectric layer, said step of forming a contact structure comprising forming a first conducting region (102; 27a) and forming a second conducting region (103; 33a) of chalcogenic material in electric contact with said
15 first conducting region;

characterized in that said step of forming said first conducting region comprises forming a strip-shaped region (102; 27a) having a longitudinal direction delimited by an end face (110) extending
20 transversely to said upper surface (92; 16);

and said step of forming a second conducting region comprises forming said second conducting region (103; 33a) in contact with said first conducting region at said end face.

10. A process according to claim (9), wherein said end face (110) has a generally rectangular shape having a height (S) comprised between 5 nm and 50 nm and a width (W) comprised between 5 nm and 50 nm.

5 11. A process according to claim 9 or 10, wherein said step of forming said first conducting region (27a) comprises depositing a first conductive layer (27) on a bottom portion (20) of said dielectric layer (20, 42); forming a delimitation layer (29) on top of said first 10 conductive layer, said delimitation layer (29) having a step (30) with a vertical side wall surface (30); forming a sacrificial portion (31a) on said vertical side wall surface; removing said first delimitation layer (29); etching said first conductive layer (27a) 15 using said a sacrificial portion (31a) as a mask; and removing said sacrificial portion.

12. A process according to claim 11, wherein said step of forming a sacrificial portion (31a) comprises depositing a sacrificial layer on said first conducting 20 region and said delimitation layer (29) and anisotropically etching said sacrificial layer (31).

13. A process according to claim 11 or 12, wherein after removing said sacrificial portion (31a), an insulating layer (30) is deposited on said first

conducting region (27a) and said bottom portion (20) of said dielectric layer (20, 42); a trench (32) is formed to remove at least a portion of said bottom portion and an end portion of said first conducting
5 region, thereby defining said end face (110); and a second conductive layer (33) of said chalcogenic material is deposited, filling said trench (32) and contacting said end face (110).

14. A process according to claim 13, comprising the
10 step of forming a PCM device (10) including a memory cell comprising a selection element (13-15) and a storage element (33b), said storage element being formed by a heater element including said first conducting region and a storage region comprising said
15 second conducting region.

15. A process according to claim 14, comprising, after depositing said second conductive layer (33), depositing an electrode layer (35) and defining said electrode layer and said second conductive layer, to
20 define a bit line (41).

ABSTRACT

A contact structure 98 for a PCM device is formed by an elongated formation 102 having a longitudinal extension parallel to the upper surface 92 of the body 91 and an end face 110 extending in a vertical plane. The end phase 110 is in contact with a bottom portion of an active region 103 of chalcogenic material so that the dimensions of the contact area defined by the end face 110 are determined by the thickness S of the elongated formation and by the width W thereof.

Figure 4

Express Mail No. EV530953239US
Appendix 2

Elena Cerbaro

Da: "Fabio Pellizzer" <fabio.pellizzer@st.com>
A: <cerbaro@studiotorta.it>
Cc: <roberto.bez@st.com>; <giorgio.pollaccia@st.com>; <roberta.radaelli@st.com>; "Osama Khouri" <Osama.KHOURI@st.com>
Data invio:
Allega: 02-AG-300.zip
Oggetto: Re: Fw: 02-AG-300/RR

Buongiorno Ing. Cerbaro.

Chiedo scusa per il colpevole ritardo.

In allegato trova il file .zip con le correzioni (solita password).

Mi faccia sapere se ci sono problemi.

Fabio

cerbaro@studiotorta.it wrote:

> ____ Ricordo che non ho ancora
> avuto vostre indicazioni e commenti sul testo inviato. Elena Cerbaro
> Studio Torta
> Tel: 0039/011/561.13.20
> __________________
> This e-mail and any attachment contain information which is private
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> not the addressee, you are not authorized to read, copy or use this
> e-mail or any attachment. If you have received this e-mail in error,
> please destroy it and notify the sender by return e-mail.

13.12.02. Telef a Radaelli – In attesa ancora di approvaz. Ovonix

8.1.03 – Radaelli – Testo già rivisto da Ovonix che ha fatto piccole modifiche. Lo sta guardando Bez. Quando dà OK depositare

From: Fabio Pellizzer <fabio.pellizzer@st.com>
To: Elena Cerbaro
Cc: roberto.bez@st.com; giorgio.pollaccia@st.com; Roberta Radaelli (ST); Osama Khouri
Sent:
Attached: 02-AG-300-1.2.zip
Subject: Re: Fw: 02-AG-300/RR

Good day Ing. Cerbaro,

Please excuse my delay.

Attached is the .zip file with the corrections (usual password).

Let me know if there are problems.

Fabio

cerbaro@studiotorta.it wrote:

> ____ I remind you that I do not yet have your
> information and comments on the text that I sent. Elena Cerbaro
> Studio Torta
> Tel: 0039/011/561.13.20

13/12/02 Telephoned Radaelli – Still waiting for the Ovonix approval
8/1/03 Radaelli – text already reviewed by Ovonix which made small changes.
Bez is reviewing it – file when he gives the OK.

Express Mail No. EV530953239US

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants : Osama Khouri et al.
Application No. : 10/756,195
Filed : January 13, 2004
For : SUBLITHOGRAPHIC CONTACT STRUCTURE, IN PARTICULAR FOR A PHASE CHANGE MEMORY CELL, AND FABRICATION PROCESS THEREOF

Examiner : Thanhha S. Pham
Art Unit : 2813
Docket No. : 854163.412

Commissioner for Patents
P.O. Box 1450
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RULE 131 DECLARATION

Commissioner for Patents:

I, Fabio Pellizzer, residing at Via Carotte, 6, Cornate d'Adda (MI), Italy, declare as follows:

I am an original, first, and joint inventor of the subject matter which is claimed and for which a patent is sought for the application identified above.

My co-inventors and I were in possession of the invention defined by the claims of the application identified above ("the present application") prior to December 13, 2002. Attached as Appendix A is a printed copy of an email sent by Elena Cerbaro, a European patent attorney, to my co-inventors and me dated prior to December 13, 2002 (see English translation included in Appendix A). The email included an attached draft patent application which describes in detail the claimed invention. For example, claims 1-15 of the draft patent application attached to the email are substantially the same as claims 1-15 of the present application. In addition, the drawings and description of the invention included in the draft

patent application attached to the email are substantially the same as those of the present application.

Attached as Appendix B is a printed copy of an email that I sent prior to December 13, 2002 to Elena Cerbaro; my co-inventors; Roberta Radaelli, who is a patent attorney in the patent department of STMicroelectronics, Srl which is one of the assignees of the present application; and Roberto Bez, who was the person in charge of the technical aspects of phase change memories at STMicroelectronics, Srl (see English translation included in Appendix B). My email included an attached draft application with minor changes compared to the draft patent application attached to the email in Appendix A.

Attached as Appendix C is a printed copy of another email, dated January 9, 2003, that I sent to Elena Cerbaro, Roberta Radaelli, my co-inventors, and Robert Bez (see English translation included in Appendix C). The email in Appendix C included an attached draft application with minor changes compared to the draft patent application attached to the email in Appendix A. As indicated in the email in Appendix C, the changes to the draft were made by Tyler Lowrey, who was a basic researcher in phase change memories and a founder of Ovonyx Inc., which is another one of the assignees of the present application.

The emails discussed above support my understanding and belief that a patent application was being diligently pursued from prior to December 13, 2002 to January 15, 2003, which is the date that European Patent Application 03425016.7 was filed for the invention claimed in the present application. In particular, because the European Patent Application was being filed on behalf of STMicroelectronics and Ovonyx, getting approval for filing the application from the necessary people at both companies required much diligence from prior to December 13, 2002 to January 15, 2003.

In summary, my co-inventors and I conceived of the claimed invention prior to December 13, 2002, and the invention was diligently reduced to practice by completing preparation and review of a draft patent application and then filing the European Patent Application No. 03425016.7 on January 15, 2003.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made

are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

28/7/2005
Date

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Appendix A

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A: <fabio.pellizzer@st.com>; <Roberto.BEZ@st.com>; <giorgio.pollaccia@st.com>
Cc: <Roberta.RADAELLI@st.com>
Data invio:
Allega: 02-AG-300.zip
Oggetto: 02-AG-300/RR

In allegato invio la bozza della descrizione e dei disegni per la domanda in oggetto, zippati e chiusi con la solita password.
Attendo vostri commenti.

Elena Cerbaro
Studio Torta
Tel: 0039/011/561.13.20

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From: Elena Cerbaro
To: fabio.pellizzer@st.com; Roberto.BEZ@st.com; giorgio.pollaccia@st.com
Cc: Roberta Radaelli (ST)
Sent:
Attached: 02-AG-300-1.2.zip
Subject: 02-AG-300/RR

Attached is the draft of the description and drawings for the subject application, zipped and locked with the usual password.
I await your comments.

Elena Cerbaro
Studio Torta
Tel: 0039/011/561.13.20

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SUBLITHOGRAPHIC CONTACT STRUCTURE, IN PARTICULAR FOR A PHASE CHANGE MEMORY CELL, AND FABRICATION PROCESS THEREOF

(02-AG-300/RR)

5 Inventors: KHOURI Osama, POLLACCIA Giorgio, PELLIZZER Fabio

The present invention relates to a sublithographic contact structure, in particular for a phase change 10 memory cell, and a fabrication process thereof.

As is known, phase change memory cells utilize a class of materials that have the unique property of being reversibly switcheable from one phase to another with measurable distinct electrical properties 15 associated with each phase. For example, these materials may change between an amorphous disordered phase and a crystalline, or polycrystalline, ordered phase. A material property that may change and provide a signature for each phase is the material resistivity, 20 which is considerably different in the two states.

At present, alloys of elements of group VI of the periodic table, such as Te or Se, referred to as chalcogenides or chalcogenic materials, can advantageously be used in phase change cells. The 25 currently most promising chalcogenide is formed by a

Ge, Sb and Te alloy ($Ge_2Sb_2Te_5$), which is currently widely used for storing information in overwritable disks.

In chalcogenides, the resistivity varies by two or
5 more magnitude orders when the material passes from the amorphous phase (more resistive) to the polycrystalline phase (more conductive) and vice versa, as shown in Figure 1. Furthermore, in the amorphous phase, resistivity strongly depends also on temperature, with
10 variations of one magnitude order every 100°C, with a behavior similar to that of P-type semiconductor materials.

Phase change may be obtained by locally increasing the temperature, as shown in Figure 2. Below 150°C both
15 phases are stable. Above 200°C (temperature of start of nucleation, designated by T_x), fast nucleation of the crystallites takes place, and, if the material is kept at the crystallization temperature for a sufficient length of time (time t_2), it changes its phase and
20 becomes crystalline. To bring the chalcogenide back into the amorphous state, it is necessary to raise the temperature above the melting temperature T_m (approximately 600°C) and then to cool the chalcogenide off rapidly (time t_1).

25 From the electrical standpoint, it is possible to

reach both critical temperatures, namely the crystallization and the melting temperatures, by causing a current to flow through a crystalline resistive element which heats the chalcogenic material
5 by the Joule effect.

The basic structure of a PCM element 1 which operates according to the principles described above is shown in Figure 3 and comprises a first electrode 2 (of resistive type, forming a heater); a programmable
10 element 3 and a second electrode 5. The programmable element 3 is made of a chalcogenide and is normally in the polycrystalline state in order to enable a good flow of current. One part of the programmable element 3 is in direct contact with the first electrode 2 and
15 forms the active portion affected by phase change, hereinafter referred to as the phase change portion 4.

In the PCM element 1 of figure 3, technological and electrical considerations impose that the contact area between the first electrode and the programmable
20 element has small dimensions, so that, for the same current density, the writing operation may be carried out at the required thermal energy with smaller current consumption.

Several proposal have been done for reducing the
25 contact area. For example, US-A-6,294,452 discloses a

process for forming a contact area of sublithographic dimensions, based on isotropically etching a polysilicon layer. The resulting sublithographic dimensions depend on the quality of the etching.

5 US 2001/0002046 discloses a process for forming an electrode of a chalcogenide switching device, wherein a spacer layer deposited in a lithographic opening is anisotropically etched and laterally defines an electrode. The resulting width of the electrode depends
10 on the thickness of a spacer layer.

Patent application 01128461.9, filed on 5.12.2001, and entitled "Small area contact region, high efficiency phase change memory cell, and manufacturing method thereof", teaches forming the contact area as an
15 intersection of two thin portions extending transversely with respect to one another and each of a sublithographic size. In order to form the thin portions, deposition of layers is adopted.

In all the indicates prior solutions, any
20 variation in the electrode width L (Figure 3), due for example to the process tolerances, affects, in a linear way, the contact area of the active region 4. Thus, the width L may have tolerances that are not acceptable as regards repeatability and uniformity of the cell
25 characteristics.

The object of the invention is thus to provide a contact region having an area less dependent on the process variations.

According to the present invention, there are
5 provided a electronic semiconductor device and a process for manufacturing an electronic semiconductor device, as defined respectively in claims 1, and 9.

According to one aspect of the invention, the contact area is formed laterally to the active region
10 and has a height and width. Advantageously, the height of the contact area is determined by the thickness of a deposited layer, which is technologically controlled and may be designed to be sublithografic. Furthermore, according to another aspect of the invention, the width
15 of the contact area is determined by the width of a spacer which may also be designed of sublithographic dimensions and may be dimensionally controlled with a good accuracy.

For the understanding of the present invention, a
20 preferred embodiment is now described, purely as a non-limitative example, with reference to the enclosed drawings, wherein:

- Figure 1 illustrates the characteristic current-voltage of a phase change material;
25 - Figure 2 shows the temperature versus current

plot of a phase change material;

- Figure 3 shows the basic structure of a PCM memory element;

- Figure 4 shows a cross section of a contact structure according to the present invention;

- Figure 5 is a perspective view of a portion of the contact structure of Figure 4 showing the variability of the contact area due to technological tolerances;

- Figure 6 is a cross-section of a PCM memory element in an initial manufacturing step;

- Figures 7-11 are cross-sections of an enlárged detail of Figure 6, in subsequent manufacturing steps;

- Figure 12 is a perspective view of the structure of Figure 11; and

- Figures 13-16 are cross-sections of the PCM memory element, in subsequent manufacturing steps, taken in a perpendicular plane with respect to Figures 7-11.

Figure 4 illustrates the basic structure of a contact structure according to the invention. In detail, an electronic device 90 has a body 91 (e.g. a substrate) of monocrystalline material defining an upper surface 92 and a lower surface 93 and accommodating electronic components 94, represented

schematically. A dielectric layer 95 extends on top of the body 91 and accommodates the contact structure, indicated at 98. The contact structure 98 is formed by a first electrode 100 and an active region 103 of
5 chalcogenic material. The first electrode 100, connected to the electronic components 94 as shown schematically for one of them, has a horizontal portion 102 adjacent to and in contact with the active region 103. A second electrode 104 is formed on the active
10 region 103 and is in electric contact therewith.

As better shown in the perspective view Figure 5, the horizontal portion 102 has an elongated shape extending along a longitudinal direction X parallel to the upper and lower surfaces 92, 93 of the body 91. The
15 horizontal portion 102 is longitudinally delimited by an end face 110. The end face 110 extends in a vertical plane, which is ideally perpendicular to the longitudinal direction X and thus to the upper and lower surfaces 92, 94 and defines a lateral contact
20 area with the active region 104. The end face 110 is here rectangular and has a height S (extending parallel to direction Z) and a width W (extending parallel to direction Y). The portion of the active region 104 adjacent to the end face 110 undergoes phase change and
25 thus corresponds to the active region 4 of Figure 3.

Because of the vertical arrangement of the end face 110 and thus of the contact area, the height S is equal to the thickness of the horizontal portion 102 of the first electrode 100, and thus may be designed to be
5 sublithographic, that is smaller than the minimum dimension obtainable through optical UV lithography.

In practice, the contact structure 98 according to Figures 4, 5 is formed by an elongated formation (horizontal portion 102 of the first electrode 100)
10 having a longitudinal extension parallel to the upper surface 92 of the body 91 and an end face 110 extending in a vertical plane and in contact with the active region 103 so that the dimensions of the contact area (defined by the end face 110) are determined by the
15 thickness S of the elongated formation and by the width W thereof.

The height S of the horizontal portion 102 and thus of the contact area is more controllable than the electrode width L of prior art contact structures
20 (Figure 3), so that PCM cells having the contact structure of Figure 4 have more uniform dimensions than prior art cells. The thickness tolerance of a conductive layer forming the horizontal portion 102 allows, for same overall dimensions, a higher
25 constructive confidence than electrodes the contact

area whereof depends on the width L.

The height S also depends on the quality of the operation used to define the end face 110, in particular by the etching operation used to this end.
5 Figure 5 shows the possible variation of the contact area in case etching does not ensure exact verticality of the end face 110, so that horizontal portion 102 has an inclined end face, indicated at 110', forming an angle α with ideal end face 110 (which, as said, is
10 perpendicular to the upper surface 92). In this case, the height S' of the inclined end face 110' is greater than height S by a quantity depending on the angle α, since

$$S' = S/\cos\alpha.$$

15 In the worst cases, with current technologies, $\alpha \leq 5°$ **(→confermare←)**, so that $\cos\alpha \cong 1$ [$\cos(5°)=0.99619$]. Since any variation of height S has the same impact on the contact area, the variation of the contact area due to process tolerances affecting
20 the height S is lower than 2% **(→confermare←)**

Furthermore, also the width W may be sublithographic, by exploiting the spacer technique, as discussed later on, with reference to Figures 7-12. This technique has a tolerance of ±10%.

25 The process for manufacturing the contact structure

of Figure 4 will be now described, with reference to Figures 6-16.

First, Figure 6, a wafer 10 comprising a P-type substrate 11 having an upper surface 16 is subjected to
5 standard front end steps. In particular, inside the substrate 11 insulation regions 12 are formed and delimit active areas; then, in succession, base regions 13 of N-type, base contact regions 14 of N^+-type, and emitter regions 15 of P^+-type are implanted. The base
10 regions 13, base contact regions 14, and emitter regions 15 form diodes or bipolar transistors that define selection elements for the memory cells.

Next, a first dielectric layer 18 is deposited and planarized; openings are formed in the first dielectric
15 layer 18 above the base contact regions 14 and emitter regions 15, and the openings are filled with tungsten to form emitter contacts 19a and base contacts 19b. Then, a second dielectric layer 20 -for example, an undoped silicon glass (USG)- is deposited, and openings
20 21, for example, cylindrical-shaped, are formed in the second dielectric layer 20 above the emitter contact 19a. Next, a cup-shaped region 22 is formed, e.g. by depositing an electrode layer, for example of TiSiN, TiAlN or TiSiC, that conformally coats the walls and
25 bottom of the openings 21 and is subsequently removed

outside the openings 21. The cup-shaped region 22 thus has a vertical wall 22a extending along the cylindrical side surface of the openings 21. The remaining portions of the electrode layer are then filled with dielectric
5 material 23.

Then, a first conductive layer 27, for instance of TiSiN, having a thickness of 20 nm **(???)**, corresponding to the desired height S of the contact area 110, thus obtaining the structure of Figure 6. As visible, the
10 first conductive layer 27 extends parallel to the upper surface 16 of substrate 11.

Next, Figure 7, a delimiting layer 29 of insulating material, for example **???**, is deposited. The delimiting layer 29 has a thickness of, for instance, 150 nm
15 **(???)**. Then, using a mask, one part of the delimiting layer 29 is removed by dry etching to form a step which has a vertical side 30 that extends vertically on top of the dielectric material 23, and crosses the vertical wall 22a of cup-shaped region 22 (at a point located
20 before or behind the drawing plane, and thus not visible in Figure 7).

Next, a sacrificial layer 31, for example nitride with a thickness of 30 nm (???), is deposited conformally. In particular, the sacrificial layer forms
25 a vertical wall 31a that extends along the vertical

side 30 of the delimiting layer 29. Thus, the structure of Figure 7 is obtained.

Thereafter (Figure 8), the sacrificial layer 31 undergoes an anisotropic etching (???) that results in
5 removal of the horizontal portions of the sacrificial layer 31 and of part of the vertical wall 31a. By appropriately choosing the thickness of the delimiting layer 29 and the thickness of the sacrificial layer 31, as well as the time and type of etching, it is possible
10 to obtain the desired sublithographic width W for the bottom part of the remaining vertical wall 31a.

Then, Figure 9, the remaining portion of the delimiting layer 29 is removed and, Figure 10, using the vertical wall 31a as a mask, the first conductive
15 layer 27 is defined. Thereafter, Figure 11, the vertical wall 31a is removed.

Now, as shown in perspective in Figure 12, the remaining portion of the first conductive layer 27 (strip-shaped portion 27a) has a height S and a width
20 W.

Thereafter, Figure 13, an insulating layer 30, e.g. of silicon oxide, and a second conductive layer 31, e.g. of Ti, are deposited in sequence.

Then, Figure 14, a trench 32 of lithographic
25 dimensions is opened. The trench 32 is an aperture

having a preset length in the direction perpendicular to the drawing sheet and intersects the strip-shaped portion 27a and extends within the second dielectric layer 20 so as to longitudinally delimit the strip-
5 shaped portion 27a. In practice, the trench 32 determines the length L1 of the strip-shaped portion 27a. **(→che cosa delimita la lunghezza L1 all'altra estremità longitudinale, non mostrata nei disegni???←)**

Thereafter, Figure 15, a chalcogenic layer 33, for
10 example of $Ge_2Sb_2Te_5$ having a thickness of e.g. ???, is conformally deposited and fills the trench 32 with a reduced area portion 33b the shape and dimensions whereof are determined by the trench 32.

Then, a barrier layer 34, for example of Ti/TiN,
15 and a metal layer 35, for example of AlCu, are deposited in sequence on top of the chalcogenic layer 33; the stack formed by the metal layer 35, the barrier layer 34 and the chalcogenic layer 33 is defined using a same mask, thus forming a bit line 41 including a
20 chalcogenic region 33a and metal regions 34a, 35a. Finally, a third dielectric layer 42 is deposited, which is opened above the base contacts 19b. The openings thus formed are filled with tungsten to form top contacts 43 in order to prolong upwards the base
25 contacts 19b. Then standard steps are performed for

forming connection lines in contact with the top contacts 43 and with the bits lines 41, pads are formed and a passivation layer 45 is deposited, defining a device main surface 46. Thus, the final structure of
5 Figure 16 is obtained.

In practice, the strip-shaped portion 27a (corresponding to the horizontal portion 102 of the first electrode 100 of Figure 4) has a longitudinal extension parallel to upper surface 16 of the substrate
10 11 and forms, with the bottom portion of the reduced area portion 33b, a contact area the height whereof is defined by the thickness of the first conductive layer 27 and the width whereof is defined by the thickness of the sacrificial layer 31. The quality of the etching of
15 trench 32 determines the orientation of the contact area with respect to the upper surface 16.

The advantages of the present invention are clear from the above. In particular, it is outlined that the present contact structure has a very good technological
20 repeatability, a lower dependence from the process variations than prior art solutions, while maintaining a very small contact area, having sublithographic dimensions in both directions.

Finally, it is clear that numerous variations and
25 modifications may be made to the contact structure and

process described and illustrated herein, all falling within the scope of the invention as defined in the attached claims. In particular, it is stressed that the direction of the horizontal portion 102 and the first
5 conductive layer 27 is defined with reference to the upper surface 92, 16 of the substrate, intending therewith a plane corresponding to the original upper surface of the wafer. In practice, the horizontal portion 102 and the first conductive layer 27 are
10 perpendicular to the direction of growing of the substrate, due to the deposition of the various superficial layers. If, due to deposition, thermal growing, etching and implant steps carried out on the wafer, the upper surface 16 of the finished device is
15 no more planar, reference may be done to the lower surface 93 of the substrate or to the device main surface 46.

CLAIMS

1. An electronic semiconductor device (90), comprising:

a body (91; 11) of semiconductor material having an
5 upper surface (92; 16);

a dielectric layer (95; 20, 42) extending on top of said body;

a contact structure (98) in said dielectric layer, said contact structure comprising a first conducting
10 region (102; 27a) and a second conducting region (103; 33a), said second conducting region being of chalcogenic material and being in electric contact with said first conducting region;

characterized in that said first conducting region
15 (102; 27a) has a strip-like shape having a longitudinal direction delimited by an end face (110) extending transversely to said upper surface (92; 16) and forming a contact area with said second conducting region (103; 33a).

20 2. A device according to claim 1, wherein said first conducting region (102; 27a) extends in a first direction (X) parallel to said upper surface (92; 16).

3. A device according to claim 1 or 2, wherein said end face (110) is perpendicular to said upper surface

(92; 16) within process tolerances.

4. A device according to any of claims 1-3, wherein said end face (110) has a generally rectangular shape having a height (S) and a width (W).

5 5. A device according to claim 4, wherein said height (S) is comprised between ??? and ??? and said width (W) is comprised between ??? and ???.

6. A device according to any of claims 1-4, forming a PCM device (10) including a memory cell comprising a
10 selection element (13-15) and a storage element, said storage element being formed by a heater element (22a, 27a) including said first conducting region (27a) and a storage region (33a) comprising said second conducting region.

15 7. A device according to claim 6, wherein said selection element (13-15) is formed in said body (11), a lower electrode (19a) extends in said dielectric layer (20, 42) between said selection element and said first conducting region (27a) and an upper electrode
20 (35a) extends in said dielectric layer on said second conducting region (33a) and forms a bit line.

8. A device according to claim 7, wherein said second conducting region (33a) has a reduced area portion (33b) in contact with said first conducting

region (27a) and an upper enlarged portion extending on top of said reduced area portion and in contact with said upper electrode (35a).

9. A process for manufacturing an electronic
5 semiconductor device (10), comprising the steps of:

providing a body (91; 11) of semiconductor material having an upper surface (92; 16);

forming a dielectric layer (95; 20, 42) extending on top of said body; and

10 forming a contact structure (98) in said dielectric layer, said step of forming a contact structure comprising forming a first conducting region (102; 27a) and forming a second conducting region (103; 33a) of chalcogenic material in electric contact with said
15 first conducting region;

characterized in that said step of forming said first conducting region comprises forming a strip-shaped region (102; 27a) having a longitudinal direction delimited by an end face (110) extending
20 transversely to said upper surface (92; 16);

and said step of forming a second conducting region comprises forming said second conducting region (103; 33a) in contact with said first conducting region at said end face.

10. A process according to claim (9), wherein said end face (110) has a generally rectangular shape having a height (S) comprised between ??? and ??? and a width (W) comprised between ??? and ???.

5 11. A process according to claim 9 or 10, wherein said step of forming said first conducting region (27a) comprises depositing a first conductive layer (27) on a bottom portion (20) of said dielectric layer (20, 42); forming a delimitation layer (29) on top of said first 10 conductive layer, said delimitation layer (29) having a step (30) with a vertical side wall surface (30); forming a sacrificial portion (31a) on said vertical side wall surface; removing said first delimitation layer (29); etching said first conductive layer (27a) 15 using said a sacrificial portion (31a) as a mask; and removing said sacrificial portion.

12. A process according to claim 11, wherein said step of forming a sacrificial portion (31a) comprises depositing a sacrificial layer on said first conducting 20 region and said delimitation layer (29) and anisotropically etching said sacrificial layer (31).

13. A process according to claim 11 or 12, wherein after removing said sacrificial portion (31a), an insulating layer (30) is deposited on said first

conducting region (27a) and said bottom portion (20) of said dielectric layer (20, 42); a trench (32) is formed to remove at least a portion of said bottom portion and an end portion of said first conducting region, thereby defining said end face (110); and a second conductive layer (33) of said chalcogenic material is deposited, filling said trench (32) and contacting said end face (110).

14. A process according to claim 13, comprising the step of forming a PCM device (10) including a memory cell comprising a selection element (13-15) and a storage element (33b), said storage element being formed by a heater element including said first conducting region and a storage region comprising said second conducting region.

15. A process according to claim 14, comprising, after depositing said second conductive layer (33), depositing an electrode layer (35) and defining said electrode layer and said second conductive layer, to define a bit line (41).

ABSTRACT

A contact structure 98 for a PCM device is formed by an elongated formation 102 having a longitudinal extension parallel to the upper surface 92 of the body 91 and an end face 110 extending in a vertical plane. The end phase 110 is in contact with a bottom portion of an active region 103 of chalcogenic material so that the dimensions of the contact area defined by the end face 110 are determined by the thickness S of the elongated formation and by the width W thereof.

Figure 4

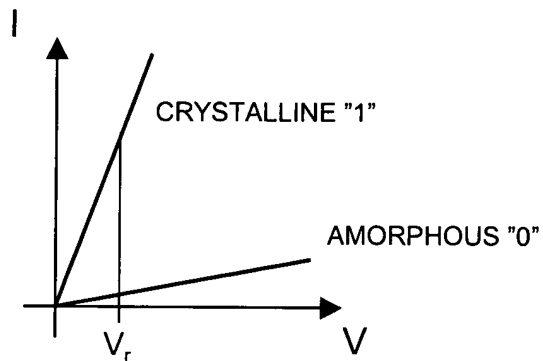


Fig.1

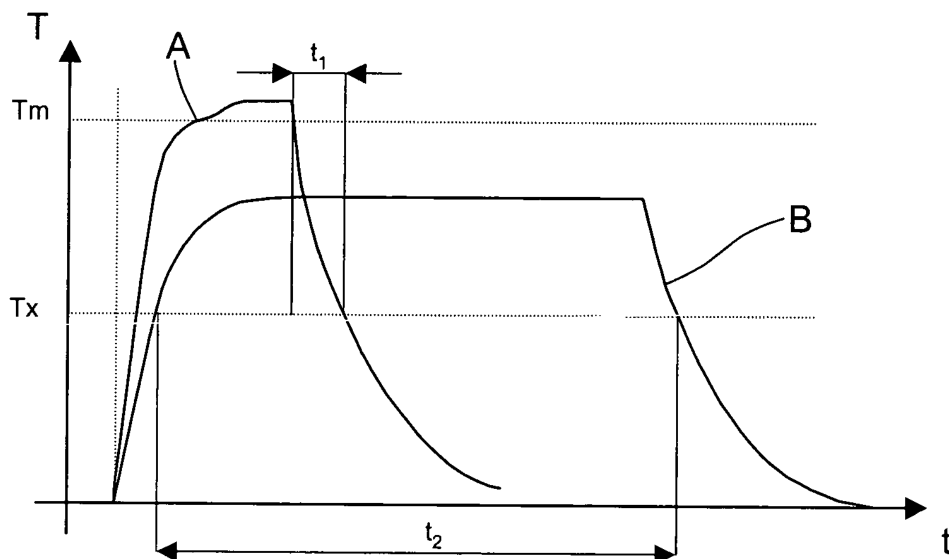


Fig.2

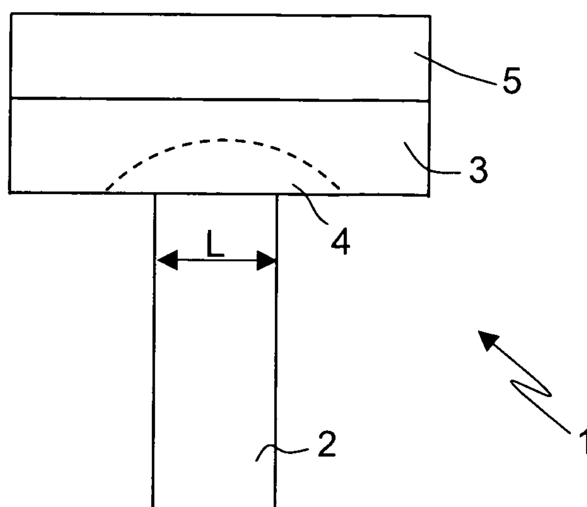


Fig.3

02-AG-300

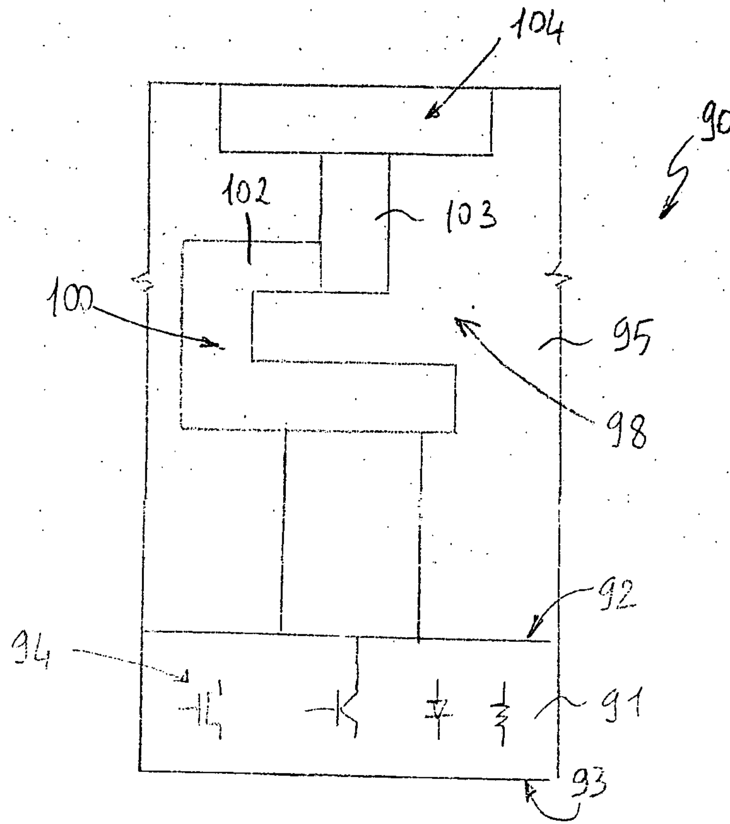
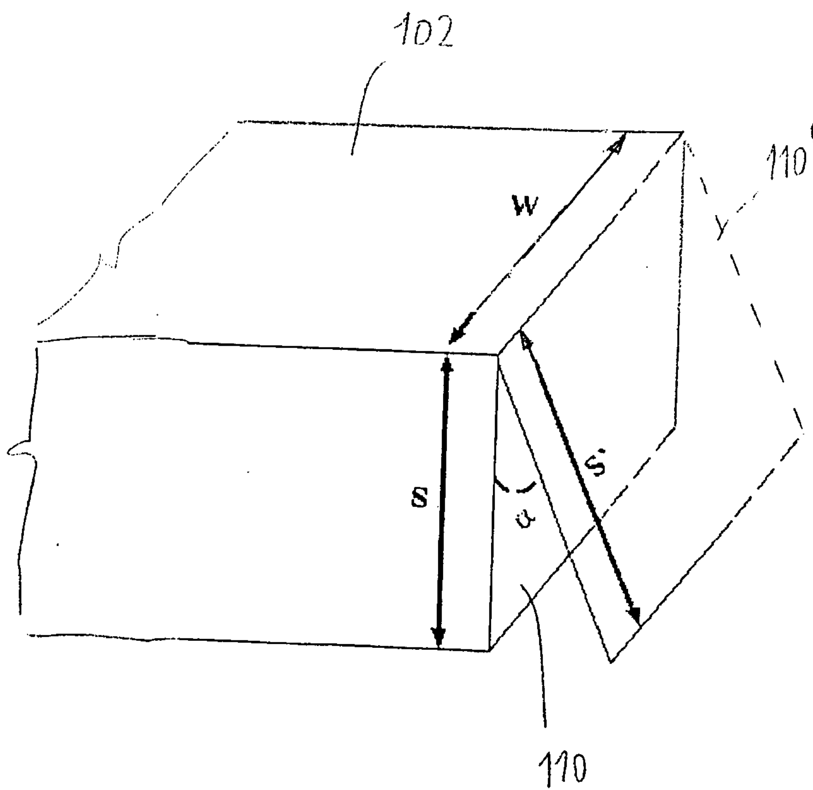


Fig 4



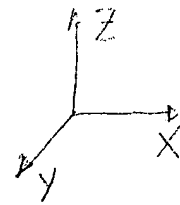


Fig.5

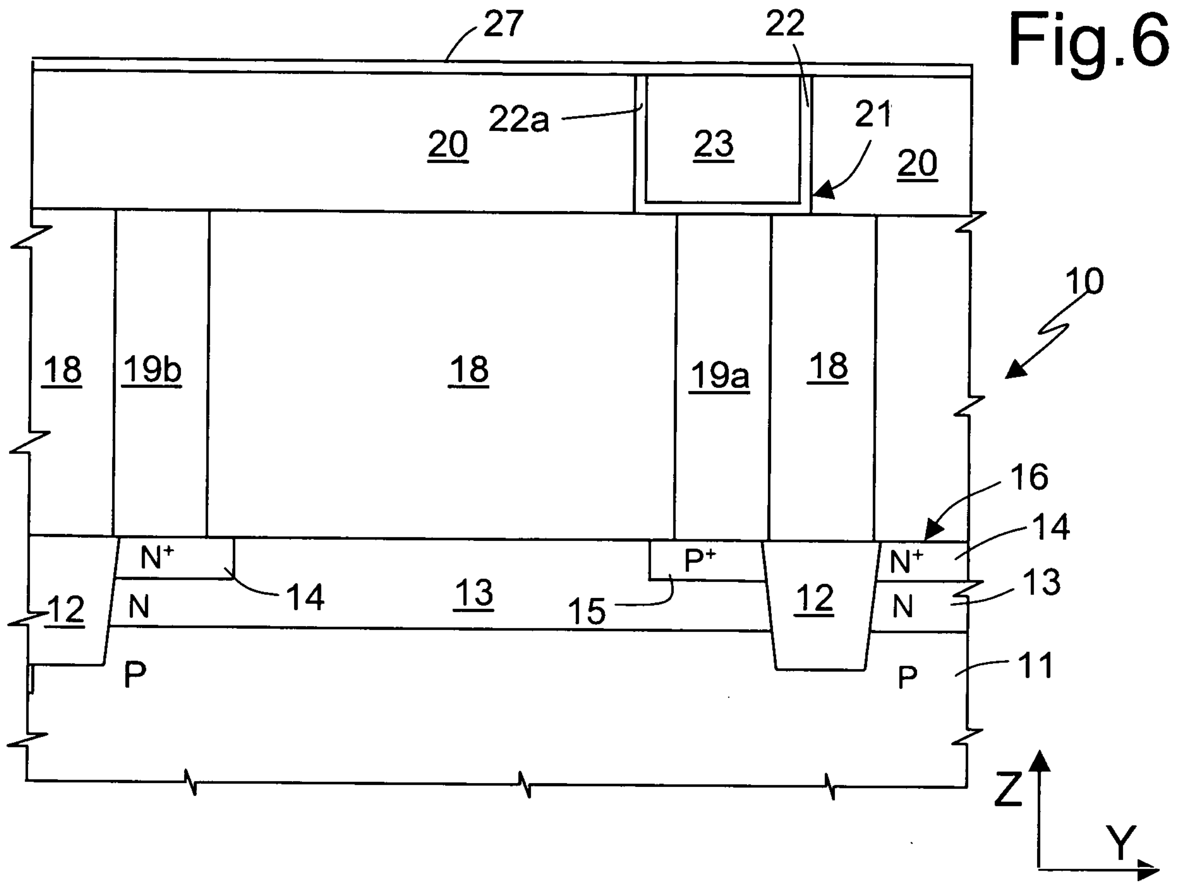
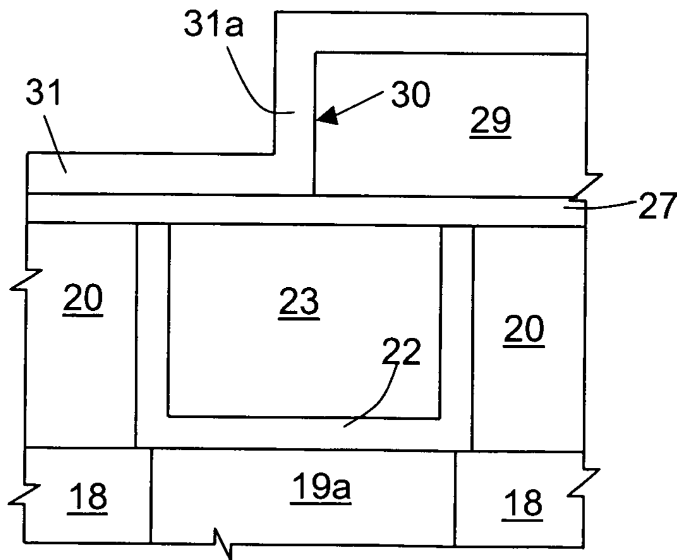


Fig.6
27
22
22a
20
23
21
20
10
18
19b
18
19a
18
16
14
N+
P+
N+
13
12
14
13
15
12
N
N
12
P
P
11
Z
Y


31a
31
30
29
27
20
23
20
22
18
19a
18
Fig.7

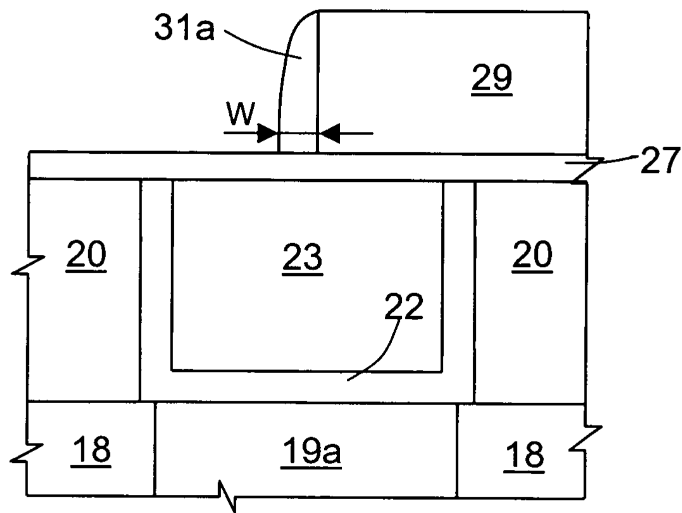


Fig.8

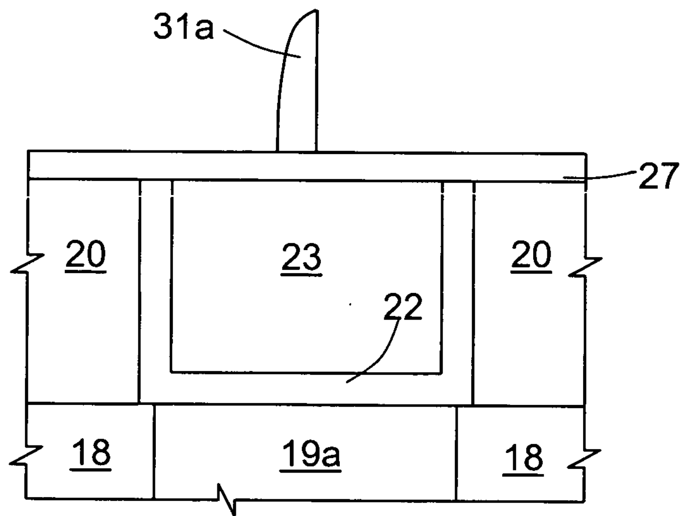


Fig.9

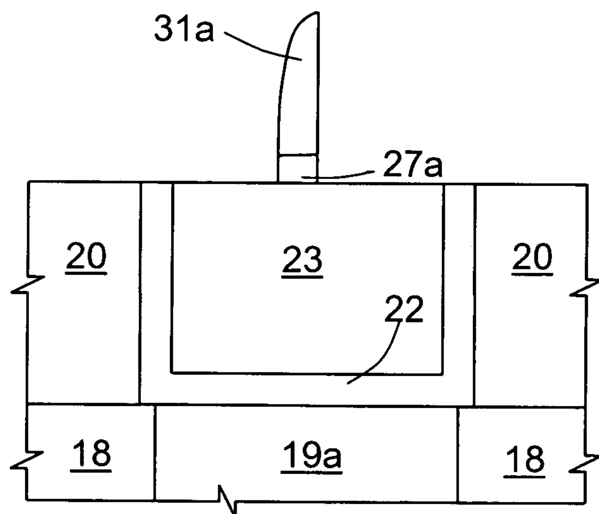


Fig.10

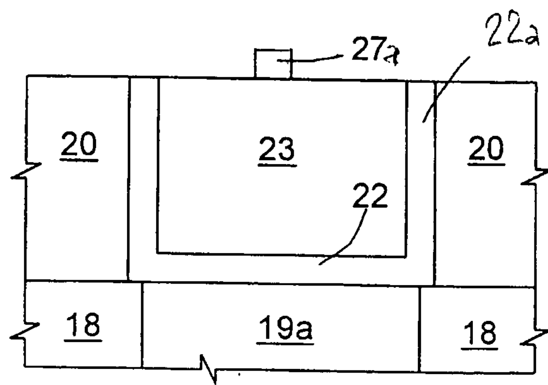


Fig.11

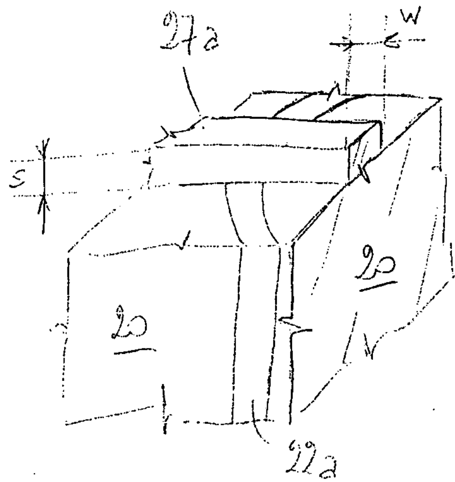
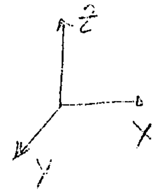


Fig. 12



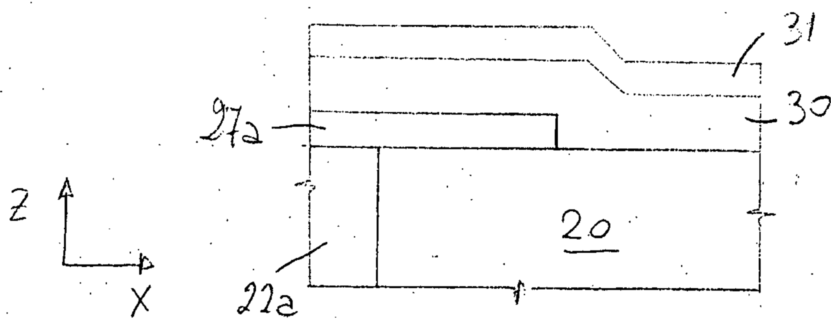


Fig. 13

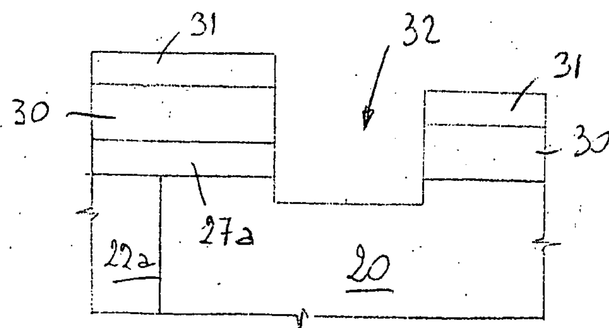


Fig. 14

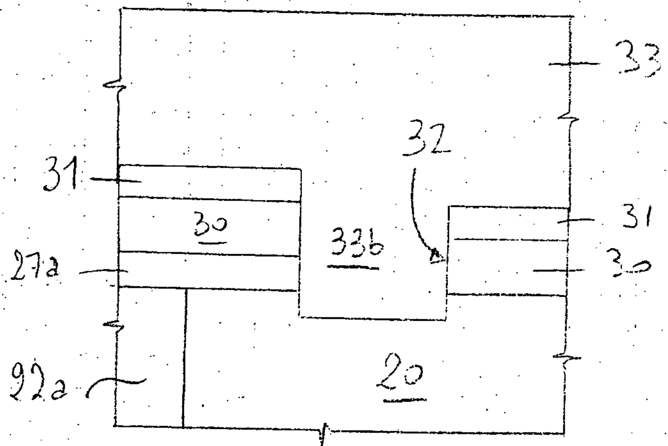


Fig. 15

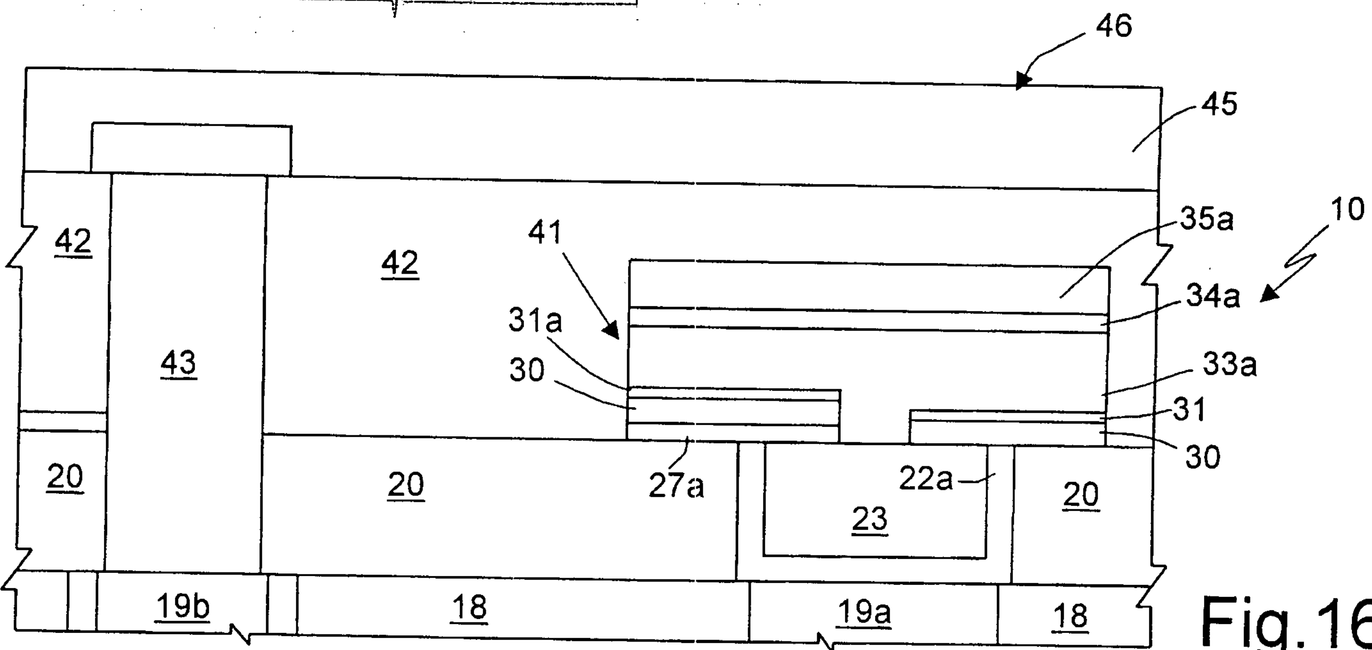


Fig.16

Express Mail No. EV530953239US
Appendix B

Elena Cerbaro

Da: "Fabio Pellizzer" <fabio.pellizzer@st.com>
A: "Elena Cerbaro" <cerbaro@studiotorta.it>
Cc: <roberto.bez@st.com>; <giorgio.pollaccia@st.com>; "Roberta Radaelli (ST)" <roberta.radaelli@st.com>; "Osama Khouri" <Osama.KHOURI@st.com>
Data invio:
Allega: 02-AG-300.zip
Oggetto: Re: Fw: 02-AG-300/RR

Buongiorno Ing. Cerbaro.

Chiedo scusa per il colpevole ritardo.

In allegato trova il file .zip con le correzioni (solita password).

Mi faccia sapere se ci sono problemi.

Fabio

cerbaro@studiotorta.it wrote:

> ____ Ricordo che non ho ancora
> avuto vostre indicazioni e commenti sul testo inviato. Elena Cerbaro
> Studio Torta
> Tel: 0039/011/561.13.20
> ________________
> This e-mail and any attachment contain information which is private
> and confidential and is intended for the addressee only. If you are
> not the addressee, you are not authorized to read, copy or use this
> e-mail or any attachment. If you have received this e-mail in error,
> please destroy it and notify the sender by return e-mail.

This email and any files transmitted with it are confidential and intended solely for the use of the individual or entity to whom they are addressed. If you have received this email in error please notify the system manager. This message contains confidential information and is intended only for the individual named. If you are not the named addressee you should not disseminate, distribute or copy this e-mail.

From: Fabio Pellizzer <fabio.pellizzer@st.com>
To: Elena Cerbaro
Cc: roberto.bez@st.com; giorgio.pollaccia@st.com; Roberta Radaelli (ST); Osama Khouri
Sent:
Attached: 02-AG-300-1.2.zip
Subject: Re: Fw: 02-AG-300/RR

Good morning Ing. Cerbaro,

Please excuse my delay.

Attached is the .zip file with the corrections (usual password).

Let me know if there are problems.

Fabio

cerbaro@studiotorta.it wrote:

> ____ I remind you that I do not yet have your
> information and comments on the text that I sent. Elena Cerbaro
> Studio Torta
> Tel: 0039/011/561.13.20 ____________________
> This e-mail and any attachment contain information which is private
> and confidential and is intended for the addressee only. If you are
> not the addressee, you are not authorized to read, copy or use this
> e-mail or any attachment. If you have received this e-mail in error,
> please destroy it and notify the sender by return e-mail.

SUBLITHOGRAPHIC CONTACT STRUCTURE, IN PARTICULAR FOR A PHASE CHANGE MEMORY CELL, AND FABRICATION PROCESS THEREOF

(02-AG-300/RR)

5 Inventors: KHOURI Osama, POLLACCIA Giorgio, PELLIZZER Fabio

The present invention relates to a sublithographic contact structure, in particular for a phase change
10 memory cell, and a fabrication process thereof.

As is known, phase change memory cells utilize a class of materials that have the unique property of being reversibly switcheable from one phase to another with measurable distinct electrical properties
15 associated with each phase. For example, these materials may change between an amorphous disordered phase and a crystalline, or polycrystalline, ordered phase. A material property that may change and provide a signature for each phase is the material resistivity,
20 which is considerably different in the two states.

At present, alloys of elements of group VI of the periodic table, such as Te or Se, referred to as chalcogenides or chalcogenic materials, can advantageously be used in phase change cells. The
25 currently most promising chalcogenide is formed by a

Ge, Sb and Te alloy ($Ge_2Sb_2Te_5$), which is currently widely used for storing information in overwritable disks.

In chalcogenides, the resistivity varies by two or more magnitude orders when the material passes from the amorphous phase (more resistive) to the polycrystalline phase (more conductive) and vice versa, as shown in Figure 1. Furthermore, in the amorphous phase, resistivity strongly depends also on temperature, with variations of one magnitude order every 100°C, with a behavior similar to that of P-type semiconductor materials.

Phase change may be obtained by locally increasing the temperature, as shown in Figure 2. Below 150°C both phases are stable. Above 200°C (temperature of start of nucleation, designated by T_x), fast nucleation of the crystallites takes place, and, if the material is kept at the crystallization temperature for a sufficient time (time t_2), it changes its phase and becomes crystalline. To bring the chalcogenide back into the amorphous state, it is necessary to raise the temperature above the melting temperature T_m (approximately 600°C) and then to cool the chalcogenide off rapidly (time t_1).

From the electrical standpoint, it is possible to

reach both critical temperatures, namely the crystallization and the melting temperatures, by causing a current to flow through a crystalline resistive element which heats the chalcogenic material by the Joule effect.

The basic structure of a PCM element 1 which operates according to the principles described above is shown in Figure 3 and comprises a first electrode 2 (of resistive type, forming a heater); a programmable element 3 and a second electrode 5. The programmable element 3 is made of a chalcogenide and is normally in the polycrystalline state in order to enable a good flow of current. One part of the programmable element 3 is in direct contact with the first electrode 2 and forms the active portion affected by phase change, hereinafter referred to as the phase change portion 4.

In the PCM element 1 of figure 3, technological and electrical considerations impose that the contact area between the first electrode and the programmable element has small dimensions, so that, for the same current density, the writing operation may be carried out at the required thermal energy with smaller current consumption.

Several proposal have been done for reducing the contact area. For example, US-A-6,294,452 discloses a

process for forming a contact area of sublithographic dimensions, based on isotropically etching a polysilicon layer. The resulting sublithographic dimensions depend on the quality of the etching.

5 US 2001/0002046 discloses a process for forming an electrode of a chalcogenide switching device, wherein a spacer layer deposited in a lithographic opening is anisotropically etched and laterally defines an electrode. The resulting width of the electrode depends 10 on the thickness of a spacer layer.

Patent application 01128461.9, filed on 5.12.2001, and entitled "Small area contact region, high efficiency phase change memory cell, and manufacturing method thereof", teaches forming the contact area as an 15 intersection of two thin portions extending transversely with respect to one another and each of a sublithographic size. In order to form the thin portions, deposition of layers is adopted.

In all the indicates prior solutions, any 20 variation in the electrode width L (Figure 3), due for example to the process tolerances, affects, in a linear way, the contact area of the active region 4. Thus, the width L may have tolerances that are not acceptable as regards repeatability and uniformity of the cell 25 characteristics.

The object of the invention is thus to provide a contact region having an area less dependent on the process variations.

According to the present invention, there are
5 provided a electronic semiconductor device and a process for manufacturing an electronic semiconductor device, as defined respectively in claims 1, and 9.

According to one aspect of the invention, the contact area is formed laterally to the active region
10 and has a height and width. Advantageously, the height of the contact area is determined by the thickness of a deposited layer, which is technologically controlled and may be designed to be sublithografic. Furthermore, according to another aspect of the invention, the width
15 of the contact area is determined by the width of a spacer which may also be designed of sublithographic dimensions and may be dimensionally controlled with a good accuracy.

For the understanding of the present invention, a
20 preferred embodiment is now described, purely as a non-limitative example, with reference to the enclosed drawings, wherein:

- Figure 1 illustrates the characteristic current-voltage of a phase change material;

25 - Figure 2 shows the temperature versus current

plot of a phase change material;

- Figure 3 shows the basic structure of a PCM memory element;

- Figure 4 shows a cross section of a contact
5 structure according to the present invention;

- Figure 5 is a perspective view of a portion of the contact structure of Figure 4 showing the variability of the contact area due to technological tolerances;

10 - Figure 6 is a cross-section of a PCM memory element in an initial manufacturing step;

- Figures 7-11 are cross-sections of an enlarged detail of Figure 6, in subsequent manufacturing steps;

- Figure 12 is a perspective view of the structure
15 of Figure 11; and

- Figures 13-16 are cross-sections of the PCM memory element, in subsequent manufacturing steps, taken in a perpendicular plane with respect to Figures 7-11.

20 Figure 4 illustrates the basic structure of a contact structure according to the invention. In detail, an electronic device 90 has a body 91 (e.g. a substrate) of monocrystalline material defining an upper surface 92 and a lower surface 93 and
25 accommodating electronic components 94, represented

schematically. A dielectric layer 95 extends on top of the body 91 and accommodates the contact structure, indicated at 98. The contact structure 98 is formed by a first electrode 100 and an active region 103 of
5 chalcogenic material. The first electrode 100, connected to the electronic components 94 as shown schematically for one of them, has a horizontal portion 102 adjacent to and in contact with the active region 103. A second electrode 104 is formed on the active
10 region 103 and is in electric contact therewith.

As better shown in the perspective view Figure 5, the horizontal portion 102 has an elongated shape extending along a longitudinal direction X parallel to the upper and lower surfaces 92, 93 of the body 91. The
15 horizontal portion 102 is longitudinally delimited by an end face 110. The end face 110 extends in a vertical plane, which is ideally perpendicular to the longitudinal direction X and thus to the upper and lower surfaces 92, 94 and defines a lateral contact
20 area with the active region 104. The end face 110 is here rectangular and has a height S (extending parallel to direction Z) and a width W (extending parallel to direction Y). The portion of the active region 104 adjacent to the end face 110 undergoes phase change and
25 thus corresponds to the active region 4 of Figure 3.

Because of the vertical arrangement of the end face 110 and thus of the contact area, the height S is equal to the thickness of the horizontal portion 102 of the first electrode 100, and thus may be designed to be sublithographic, that is smaller than the minimum dimension obtainable through optical UV lithography.

In practice, the contact structure 98 according to Figures 4, 5 is formed by an elongated formation (horizontal portion 102 of the first electrode 100) having a longitudinal extension parallel to the upper surface 92 of the body 91 and an end face 110 extending in a vertical plane and in contact with the active region 103 so that the dimensions of the contact area (defined by the end face 110) are determined by the thickness S of the elongated formation and by the width W thereof.

The height S of the horizontal portion 102 and thus of the contact area is more controllable than the electrode width L of prior art contact structures (Figure 3), so that PCM cells having the contact structure of Figure 4 have more uniform dimensions than prior art cells. The thickness tolerance of a conductive layer forming the horizontal portion 102 allows, for same overall dimensions, a higher constructive confidence than electrodes the contact

area whereof depends on the width L.

The height S also depends on the quality of the operation used to define the end face 110, in particular by the etching operation used to this end. Figure 5 shows the possible variation of the contact area in case etching does not ensure exact verticality of the end face 110, so that horizontal portion 102 has an inclined end face, indicated at 110', forming an angle α with ideal end face 110 (which, as said, is perpendicular to the upper surface 92). In this case, the height S' of the inclined end face 110' is greater than height S by a quantity depending on the angle α, since

$$S' = S/\cos\alpha.$$

In the worst cases, with current technologies, $\alpha \leq 5°$, so that $\cos\alpha \cong 1$ [$\cos(5°)=0.99619$]. Since any variation of height S has the same impact on the contact area, the variation of the contact area due to process tolerances affecting the height S is lower than 2%.

Furthermore, also the width W may be sublithographic, by exploiting the spacer technique, as discussed later on, with reference to Figures 7-12. This technique has a tolerance of ±10%.

The process for manufacturing the contact structure

of Figure 4 will be now described, with reference to Figures 6-16.

First, Figure 6, a wafer 10 comprising a P-type substrate 11 having an upper surface 16 is subjected to
5 standard front end steps. In particular, inside the substrate 11 insulation regions 12 are formed and delimit active areas; then, in succession, base regions 13 of N-type, base contact regions 14 of N^+-type, and emitter regions 15 of P^+-type are implanted. The base
10 regions 13, base contact regions 14, and emitter regions 15 form diodes or bipolar transistors that define selection elements for the memory cells.

Next, a first dielectric layer 18 is deposited and planarized; openings are formed in the first dielectric
15 layer 18 above the base contact regions 14 and emitter regions 15, and the openings are filled with tungsten to form emitter contacts 19a and base contacts 19b. Then, a second dielectric layer 20 -for example, an undoped silicon glass (USG)- is deposited, and openings
20 21, for example, cylindrical-shaped, are formed in the second dielectric layer 20 above the emitter contact 19a. Next, a cup-shaped region 22 is formed, e.g. by depositing an electrode layer, for example of TiSiN, TiAlN or TiSiC, that conformally coats the walls and
25 bottom of the openings 21 and is subsequently removed

outside the openings 21. The cup-shaped region 22 thus has a vertical wall 22a extending along the cylindrical side surface of the openings 21. The remaining portions of the electrode layer are then filled with dielectric
5 material 23.

Then, a first conductive layer 27 (for instance TaSiN, TiSiN, TiN, TiAlN, etc.) having a thickness of 5-50 nm, corresponding to the desired height S of the contact area 110, thus obtaining the structure of
10 Figure 6. As visible, the first conductive layer 27 extends parallel to the upper surface 16 of substrate 11.

At this point, a mask is exposed and the conductive layer 27 is selectively etched in order to form stripes
15 parallel to the y-direction.

The width of these stripes has to be enough to touch the conductive ring on one side and to be cut by the trench etch described in Fig.14 on the other side.

Next, Figure 7, a delimiting layer 29 of insulating
20 material, for example **oxide**, is deposited. The delimiting layer 29 has a thickness of, for instance, 20-200 nm. Then, using a mask, one part of the delimiting layer 29 is removed by dry etching to form a step which has a vertical side 30 that extends
25 vertically on top of the dielectric material 23, and

crosses the vertical wall 22a of cup-shaped region 22 (at a point located before or behind the drawing plane, and thus not visible in Figure 7).

Next, a sacrificial layer 31, for example nitride
5 with a thickness of 5-50 nm, is deposited conformally. In particular, the sacrificial layer forms a vertical wall 31a that extends along the vertical side 30 of the delimiting layer 29. Thus, the structure of Figure 7 is obtained.

10 Thereafter (Figure 8), the sacrificial layer 31 undergoes an anisotropic etching that results in removal of the horizontal portions of the sacrificial layer 31 and of part of the vertical wall 31a. By appropriately choosing the thickness of the delimiting
15 layer 29 and the thickness of the sacrificial layer 31, as well as the time and type of etching, it is possible to obtain the desired sublithographic width W for the bottom part of the remaining vertical wall 31a.

Then, Figure 9, the remaining portion of the
20 delimiting layer 29 is removed and, Figure 10, using the vertical wall 31a as a hard mask, the first conductive layer 27 is defined. Thereafter, Figure 11, the vertical wall 31a is removed.

Now, as shown in perspective in Figure 12, the
25 remaining portion of the first conductive layer 27

(strip-shaped portion 27a) has a height S and a width W.

Thereafter, Figure 13, an insulating layer 30 (e.g. silicon oxide) and a second adhesion layer 31 (e.g. Si,
5 Ti, Ta, etc.) are deposited in sequence.

Then, Figure 14, a trench 32 of lithographic dimensions is opened. The trench 32 is an aperture having a preset length in the direction perpendicular to the drawing sheet and intersects the strip-shaped
10 portion 27a and extends within the second dielectric layer 20 so as to longitudinally delimit the strip-shaped portion 27a. In practice, the trench 32 determines the length L1 of the strip-shaped portion 27a.

15 Thereafter, Figure 15, a chalcogenic layer 33, for example of $Ge_2Sb_2Te_5$ having a thickness of e.g. ???, is conformally deposited and fills the trench 32 with a reduced area portion 33b the shape and dimensions whereof are determined by the trench 32.

20 Then, a barrier layer 34, for example of Ti/TiN, and a metal layer 35, for example of AlCu, are deposited in sequence on top of the chalcogenic layer 33; the stack formed by the metal layer 35, the barrier layer 34 and the chalcogenic layer 33 is defined using
25 a same mask, thus forming a bit line 41 including a

chalcogenic region 33a and metal regions 34a, 35a. Finally, a third dielectric layer 42 is deposited, which is opened above the base contacts 19b. The openings thus formed are filled with tungsten to form
5 top contacts 43 in order to prolong upwards the base contacts 19b. Then standard steps are performed for forming connection lines in contact with the top contacts 43 and with the bits lines 41, pads are formed and a passivation layer 45 is deposited, defining a
10 device main surface 46. Thus, the final structure of Figure 16 is obtained.

In practice, the strip-shaped portion 27a (corresponding to the horizontal portion 102 of the first electrode 100 of Figure 4) has a longitudinal
15 extension parallel to upper surface 16 of the substrate 11 and forms, with the bottom portion of the reduced area portion 33b, a contact area the height whereof is defined by the thickness of the first conductive layer 27 and the width whereof is defined by the thickness of
20 the sacrificial layer 31. The quality of the etching of trench 32 determines the orientation of the contact area with respect to the upper surface 16.

The advantages of the present invention are clear from the above. In particular, it is outlined that the
25 present contact structure has a very good technological

repeatability, a lower dependence from the process variations than prior art solutions, while maintaining a very small contact area, having sublithographic dimensions in both directions.

5 Finally, it is clear that numerous variations and modifications may be made to the contact structure and process described and illustrated herein, all falling within the scope of the invention as defined in the attached claims.

10 In particular, it is stressed that the direction of the horizontal portion 102 and the first conductive layer 27 is defined with reference to the upper surface 92, 16 of the substrate, intending therewith a plane corresponding to the original upper surface of the 15 wafer. In practice, the horizontal portion 102 and the first conductive layer 27 are perpendicular to the direction of growing of the substrate, due to the deposition of the various superficial layers. If, due to deposition, thermal growing, etching and implant 20 steps carried out on the wafer, the upper surface 16 of the finished device is no more planar, reference may be done to the lower surface 93 of the substrate or to the device main surface 46.

Moreover we propose an alternative embodiment of 25 the present invention in which the conductive layer 27

is in direct contact with the conductive layer 19a, thus avoiding the dielectric layers 20 and 23 and the conductive layer 22.

CLAIMS

1. An electronic semiconductor device (90), comprising:

a body (91; 11) of semiconductor material having an
5 upper surface (92; 16);

a dielectric layer (95; 20, 42) extending on top of said body;

a contact structure (98) in said dielectric layer, said contact structure comprising a first conducting
10 region (102; 27a) and a second conducting region (103; 33a), said second conducting region being of chalcogenic material and being in electric contact with said first conducting region;

characterized in that said first conducting region
15 (102; 27a) has a strip-like shape having a longitudinal direction delimited by an end face (110) extending transversely to said upper surface (92; 16) and forming a contact area with said second conducting region (103; 33a).

20 2. A device according to claim 1, wherein said first conducting region (102; 27a) extends in a first direction (X) parallel to said upper surface (92; 16).

3. A device according to claim 1 or 2, wherein said end face (110) is perpendicular to said upper surface

(92; 16) within process tolerances.

4. A device according to any of claims 1-3, wherein said end face (110) has a generally rectangular shape having a height (S) and a width (W).

5 5. A device according to claim 4, wherein said height (S) is comprised between 5 nm and 50 nm and said width (W) is comprised between 5 nm and 50 nm.

6. A device according to any of claims 1-4, forming a PCM device (10) including a memory cell comprising a 10 selection element (13-15) and a storage element, said storage element being formed by a heater element (22a, 27a) including said first conducting region (27a) and a storage region (33a) comprising said second conducting region.

15 7. A device according to claim 6, wherein said selection element (13-15) is formed in said body (11), a lower electrode (19a) extends in said dielectric layer (20, 42) between said selection element and said first conducting region (27a) and an upper electrode 20 (35a) extends in said dielectric layer on said second conducting region (33a) and forms a bit line.

8. A device according to claim 7, wherein said second conducting region (33a) has a reduced area portion (33b) in contact with said first conducting

region (27a) and an upper enlarged portion extending on top of said reduced area portion and in contact with said upper electrode (35a).

9. A process for manufacturing an electronic
5 semiconductor device (10), comprising the steps of:

providing a body (91; 11) of semiconductor material having an upper surface (92; 16);

forming a dielectric layer (95; 20, 42) extending on top of said body; and

10 forming a contact structure (98) in said dielectric layer, said step of forming a contact structure comprising forming a first conducting region (102; 27a) and forming a second conducting region (103; 33a) of chalcogenic material in electric contact with said
15 first conducting region;

characterized in that said step of forming said first conducting region comprises forming a strip-shaped region (102; 27a) having a longitudinal direction delimited by an end face (110) extending
20 transversely to said upper surface (92; 16);

and said step of forming a second conducting region comprises forming said second conducting region (103; 33a) in contact with said first conducting region at said end face.

10. A process according to claim (9), wherein said end face (110) has a generally rectangular shape having a height (S) comprised between 5 nm and 50 nm and a width (W) comprised between 5 nm and 50 nm.

5 11. A process according to claim 9 or 10, wherein said step of forming said first conducting region (27a) comprises depositing a first conductive layer (27) on a bottom portion (20) of said dielectric layer (20, 42); forming a delimitation layer (29) on top of said first
10 conductive layer, said delimitation layer (29) having a step (30) with a vertical side wall surface (30); forming a sacrificial portion (31a) on said vertical side wall surface; removing said first delimitation layer (29); etching said first conductive layer (27a)
15 using said a sacrificial portion (31a) as a mask; and removing said sacrificial portion.

12. A process according to claim 11, wherein said step of forming a sacrificial portion (31a) comprises depositing a sacrificial layer on said first conducting
20 region and said delimitation layer (29) and anisotropically etching said sacrificial layer (31).

13. A process according to claim 11 or 12, wherein after removing said sacrificial portion (31a), an insulating layer (30) is deposited on said first

conducting region (27a) and said bottom portion (20) of said dielectric layer (20, 42); a trench (32) is formed to remove at least a portion of said bottom portion and an end portion of said first conducting region, thereby defining said end face (110); and a second conductive layer (33) of said chalcogenic material is deposited, filling said trench (32) and contacting said end face (110).

14. A process according to claim 13, comprising the step of forming a PCM device (10) including a memory cell comprising a selection element (13-15) and a storage element (33b), said storage element being formed by a heater element including said first conducting region and a storage region comprising said second conducting region.

15. A process according to claim 14, comprising, after depositing said second conductive layer (33), depositing an electrode layer (35) and defining said electrode layer and said second conductive layer, to define a bit line (41).

ABSTRACT

A contact structure 98 for a PCM device is formed by an elongated formation 102 having a longitudinal extension parallel to the upper surface 92 of the body 91 and an end face 110 extending in a vertical plane. The end phase 110 is in contact with a bottom portion of an active region 103 of chalcogenic material so that the dimensions of the contact area defined by the end face 110 are determined by the thickness S of the elongated formation and by the width W thereof.

Figure 4

Express Mail No. EV530953239US
Appendix C

Elena Cerbaro

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Cc:	"Roberta Enrica RADAELLI" <roberta.radaelli@st.com>; "Roberto Bez" <Roberto.BEZ@st.com>; "Giorgio Pollaccia" <Giorgio.POLLACCIA@st.com>; "Osama Khouri" <Osama.KHOURI@st.com>
Data invio:	giovedì 9 gennaio 2003 18.54
Allega:	02-AG-300-1.2.zip
Oggetto:	02-AG-300 - Revisione con correzioni di Tyler Lowrey

Ri-buonasera Ing. Cerbaro!

Eccole anche il file .zip con la revisione finale del testo relativo
alla proposta 02-AG-300 (solita password).
Le correzioni di Tyler Lowrey sono un po' di piu' stavolta, ma niente di
drammatico.
Sono ovviamente a disposizione per eventuali chiarimenti.

Cordiali saluti.

Fabio

From: Fabio Pellizzer <:fabio.pellizzer@st.com>
To: Elena Cerbaro
Cc: Roberta Radaelli (ST); Roberto Bez; Giorgio Pollaccia; Osama Khouri
Sent: Thursday, January 09, 2003 18.54
Attached: 02-AG-300-1.2.zip
Subject: 02-AG-300 – Revision with Tyler Lowrey's corrections

Good evening again Ing. Cerbaro!

Here is the .zip file with the final revision of the text for the proposal 02-AG-300 (usual password).
Tyler Lowrey's corrections were a bit more this time, but nothing dramatic.
I'm obviously at your disposal for any clarifications.

Best wishes.

Fabio

SUBLITHOGRAPHIC CONTACT STRUCTURE, IN PARTICULAR FOR A PHASE CHANGE MEMORY CELL, AND FABRICATION PROCESS THEREOF

(02-AG-300/RR)

5 Inventors: KHOURI Osama, POLLACCIA Giorgio, PELLIZZER Fabio

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As is known, phase change memory cells utilize a class of materials that have the unique property of being reversibly switchable from one phase to another with measurable distinct electrical properties 15 associated with each phase. For example, these materials may change between an amorphous disordered phase and a crystalline, or polycrystalline, ordered phase. A material property that may change and provide a signature for each phase is the material resistivity, 20 which is considerably different in the two states.

At present, alloys of elements of group VI of the periodic table, such as Te or Se, referred to as chalcogenides or chalcogenic materials, can advantageously be used in phase change cells. The 25 currently most promising chalcogenide is formed by a

Ge, Sb and Te alloy ($Ge_2Sb_2Te_5$), which is currently widely used for storing information in overwritable disks.

In chalcogenides, the resistivity varies by two or 5 more magnitude orders when the material passes from the amorphous phase (more resistive) to the polycrystalline phase (more conductive) and vice versa, as shown in Figure 1. Furthermore, in the amorphous phase, resistivity strongly depends also on temperature, with 10 variations of one magnitude order every 100°C, with a behavior similar to that of P-type semiconductor materials.

Phase change may be obtained by locally increasing the temperature, as shown in Figure 2. Below 150°C both 15 phases are stable. Above 200°C (temperature of start of nucleation, designated by T_x), fast nucleation of the crystallites takes place, and, if the material is kept at the crystallization temperature for a sufficient time (time t_2), it changes its phase and becomes 20 crystalline. To bring the chalcogenide back into the amorphous state, it is necessary to raise the temperature above the melting temperature T_m (approximately 600°C) and then to cool the chalcogenide off rapidly (time t_1).

25 From the electrical standpoint, it is possible to

reach both critical temperatures, namely the crystallization and the melting temperatures, by causing a current to flow through a resistive element which heats the chalcogenic material by the Joule effect.

The basic structure of a PCM element 1 which operates according to the principles described above is shown in Figure 3 and comprises a first electrode 2 (of resistive type, forming a heater); a programmable element 3 and a second electrode 5. The programmable element 3 is made of a chalcogenide and is normally in the polycrystalline state after processing. One part of the programmable element 3 is in direct contact with the first electrode 2 and forms the active portion affected by phase change, hereinafter referred to as the phase change portion 4.

In the PCM element 1 of figure 3, technological and electrical considerations impose that the contact area between the first electrode and the programmable element has small dimensions, so that, for the same current density, the writing operation may be carried out at the required local thermal energy with smaller current consumption.

Several proposals have been presented for reducing the contact area. For example, US-A-6,294,452 discloses

a process for forming a contact area of sublithographic dimensions, based on isotropically etching a polysilicon layer. The resulting sublithographic dimensions depend on the quality of the etching.

5 US 2001/0002046 discloses a process for forming an electrode of a chalcogenide switching device, wherein a spacer layer deposited in a lithographic opening is anisotropically etched and laterally defines an electrode. The resulting width of the electrode depends 10 on the thickness of a spacer layer.

Patent application 01128461.9, filed on 5.12.2001, and entitled "Small area contact region, high efficiency phase change memory cell, and manufacturing method thereof", teaches forming the contact area as an 15 intersection of two thin portions extending transversely with respect to one another and each of a sublithographic size. In order to form the thin portions, deposition of layers is adopted.

In all the indicated prior solutions, any 20 variation in the electrode width L (Figure 3), due for example to the process tolerances, affects, in a linear way, the contact area of the active region 4. Thus, the width L may have tolerances that are not acceptable as regards repeatability and uniformity of the cell 25 characteristics.

The object of the invention is thus to provide a contact region having an area less dependent on the process variations.

According to the present invention, there are
5 provided an electronic semiconductor device and a process for manufacturing an electronic semiconductor device, as defined respectively in claims 1, and 9.

According to one aspect of the invention, the contact area is formed laterally to the active region
10 and has a height and width. Advantageously, the height of the contact area is determined by the thickness of a deposited layer, which is technologically controlled and may be designed to be sublithographic. Furthermore, according to another aspect of the invention, the width
15 of the contact area is determined by the width of a spacer which may also be designed of sublithographic dimensions and may be dimensionally controlled with a good accuracy.

For the understanding of the present invention, a
20 preferred embodiment is now described, purely as a non-limitative example, with reference to the enclosed drawings, wherein:

- Figure 1 illustrates the characteristic low field current-voltage of a phase change material;
25 - Figure 2 shows the temperature versus time plot

of a phase change material;

- Figure 3 shows the basic structure of a PCM memory element;

- Figure 4 shows a cross section of a contact
5 structure according to the present invention;

- Figure 5 is a perspective view of a portion of the contact structure of Figure 4 showing the variability of the contact area due to technological tolerances;

10 - Figure 6 is a cross-section of a PCM memory element in an initial manufacturing step;

- Figures 7-11 are cross-sections of an enlarged detail of Figure 6, in subsequent manufacturing steps;

- Figure 12 is a perspective view of the structure
15 of Figure 11; and

- Figures 13-16 are cross-sections of the PCM memory element, in subsequent manufacturing steps, taken in a perpendicular plane with respect to Figures 7-11.

20 Figure 4 illustrates the basic structure of a contact structure according to the invention. In detail, an electronic device 90 has a body 91 (e.g. a substrate) of monocrystalline material defining an upper surface 92 and a lower surface 93 and
25 accommodating electronic components 94, represented

schematically. A dielectric layer 95 extends on top of the body 91 and accommodates the contact structure, indicated at 98. The contact structure 98 is formed by a first electrode 100 and an active region 103 of
5 chalcogenic material. The first electrode 100, connected to the electronic components 94 as shown schematically for one of them, has a horizontal portion 102 adjacent to and in contact with the active region 103. A second electrode 104 is formed on the active
10 region 103 and is in electric contact therewith.

As better shown in the perspective view Figure 5, the horizontal portion 102 has an elongated shape extending along a longitudinal direction X parallel to the upper and lower surfaces 92, 93 of the body 91. The
15 horizontal portion 102 is longitudinally delimited by an end face 110. The end face 110 extends in a vertical plane, which is ideally perpendicular to the longitudinal direction X and thus to the upper and lower surfaces 92, 94 and defines a lateral contact
20 area with the active region 104. The end face 110 is here rectangular and has a height S (extending parallel to direction Z) and a width W (extending parallel to direction Y). The portion of the active region 104 adjacent to the end face 110 undergoes phase change and
25 thus corresponds to the active region 4 of Figure 3.

Because of the vertical arrangement of the end face 110 and thus of the contact area, the height S is equal to the thickness of the horizontal portion 102 of the first electrode 100, and thus may be designed to be
5 sublithographic, that is smaller than the minimum dimension obtainable through optical UV lithography.

In practice, the contact structure 98 according to Figures 4, 5 is formed by an elongated formation (horizontal portion 102 of the first electrode 100)
10 having a longitudinal extension parallel to the upper surface 92 of the body 91 and an end face 110 extending in a vertical plane and in contact with the active region 103 so that the dimensions of the contact area (defined by the end face 110) are determined by the
15 thickness S of the elongated formation and by the width W thereof.

The height S of the horizontal portion 102 and thus of the contact area is more controllable than the electrode width L of prior art contact structures
20 (Figure 3), so that PCM cells having the contact structure of Figure 4 have more uniform dimensions than prior art cells. The thickness tolerance of a conductive layer forming the horizontal portion 102 allows, for same overall dimensions, a higher
25 constructive confidence than electrodes the contact

area whereof depends on the width L.

The height S also depends on the quality of the operation used to define the end face 110, in particular by the etching operation used to this end.
5 Figure 5 shows the possible variation of the contact area in case etching does not ensure exact verticality of the end face 110, so that horizontal portion 102 has an inclined end face, indicated at 110', forming an angle α with ideal end face 110 (which, as said, is
10 perpendicular to the upper surface 92). In this case, the height S' of the inclined end face 110' is greater than height S by a quantity depending on the angle α, since

$$S' = S/\cos\alpha.$$

15 In the worst cases, with current technologies, $\alpha \leq 5°$, so that $\cos\alpha \cong 1$ [$\cos(5°)=0.99619$]. Since any variation of height S has the same impact on the contact area, the variation of the contact area due to process tolerances affecting the height S is lower than
20 2%.

Furthermore, also the width W may be sublithographic, by exploiting the spacer technique, as discussed later on, with reference to Figures 7-12. This technique has a tolerance of ±10%.

25 The process for manufacturing the contact structure

of Figure 4 will be now described, with reference to Figures 6-16.

First, Figure 6, a wafer 10 comprising a P-type substrate 11 having an upper surface 16 is subjected to
5 standard front end steps. In particular, inside the substrate 11 insulation regions 12 are formed and delimit active areas; then, in succession, base regions 13 of N-type, base contact regions 14 of N^+-type, and emitter regions 15 of P^+-type are implanted. The base
10 regions 13, base contact regions 14, and emitter regions 15 form diodes or bipolar transistors that define selection elements for the memory cells.

Next, a first dielectric layer 18 is deposited and planarized; openings are formed in the first dielectric
15 layer 18 above the base contact regions 14 and emitter regions 15, and the openings are filled with tungsten to form emitter contacts 19a and base contacts 19b. Then, a second dielectric layer 20 -for example, an undoped silicon glass (USG)- is deposited, and openings
20 21, for example, cylindrical-shaped, are formed in the second dielectric layer 20 above the emitter contact 19a. Next, a cup-shaped region 22 is formed, e.g. by depositing an electrode layer, for example of TiSiN, TiAlN or TiSiC, that conformally coats the walls and
25 bottom of the openings 21, a dielectric material is

then deposited filling the openings 21, and then the dielectric material and electrode layer are subsequently removed outside the openings 21, using conventional planarization techniques such as Chemical
5 Mechanical Polishing (CMP). The cup-shaped region 22 thus has a vertical wall 22a extending along the cylindrical side surface of the openings 21.

Then, a first conductive layer 27 (for instance TaSiN, TiSiN, TiN, TiAlN, etc.) having a thickness of
10 5-50 nm, corresponding to the desired height S of the contact area 110 is deposited, thus obtaining the structure of Figure 6. As visible, the first conductive layer 27 extends parallel to the upper surface 16 of substrate 11.

15 At this point, a mask is exposed and the conductive layer 27 is selectively etched in order to form stripes parallel to the y-direction.

The width of these stripes has to be enough to touch the conductive ring on one side and to be cut by
20 the trench etch described in Fig.14 on the other side.

Next, Figure 7, a delimiting layer 29 of insulating material, for example **oxide,** is deposited. The delimiting layer 29 has a thickness of, for instance, 20-200 nm. Then, using a mask, one part of the
25 delimiting layer 29 is removed by dry etching to form a

step which has a vertical side 30 that extends vertically on top of the dielectric material 23, and crosses the vertical wall 22a of cup-shaped region 22 (at a point located before or behind the drawing plane, 5 and thus not visible in Figure 7).

Next, a sacrificial layer 31, for example nitride with a thickness of 5-50 nm, is deposited conformally. In particular, the sacrificial layer forms a vertical wall 31a that extends along the vertical side 30 of the 10 delimiting layer 29. Thus, the structure of Figure 7 is obtained.

Thereafter (Figure 8), the sacrificial layer 31 undergoes an anisotropic etching that results in removal of the horizontal portions of the sacrificial 15 layer 31 and of part of the vertical wall 31a. By appropriately choosing the thickness of the delimiting layer 29 and the thickness of the sacrificial layer 31, as well as the time and type of etching, it is possible to obtain the desired sublithographic width W for the 20 bottom part of the remaining vertical wall 31a.

Then, Figure 9, the remaining portion of the delimiting layer 29 is removed and, Figure 10, using the vertical wall 31a as a hard mask, the first conductive layer 27 is defined. Thereafter, Figure 11, 25 the vertical wall 31a is removed.

Now, as shown in perspective in Figure 12, the remaining portion of the first conductive layer 27 (strip-shaped portion 27a) has a height S and a width W.

5 Thereafter, Figure 13, an insulating layer 30 (e.g. silicon oxide) and a second adhesion layer 31 (e.g. Si, Ti, Ta, etc.) are deposited in sequence.

Then, Figure 14, a trench 32 of lithographic dimensions is opened. The trench 32 is an aperture 10 having a preset length in the direction perpendicular to the drawing sheet and intersects the strip-shaped portion 27a and extends within the second dielectric layer 20 so as to longitudinally delimit the strip-shaped portion 27a. In practice, the trench 32 15 determines the length L1 of the strip-shaped portion 27a.

Thereafter, Figure 15, a chalcogenic layer 33, for example of $Ge_2Sb_2Te_5$ having a thickness of e.g. ???, is conformally deposited and fills the trench 32 with a 20 reduced area portion 33b the shape and dimensions whereof are determined by the trench 32.

Then, a barrier layer 34, for example of Ti/TiN, and a metal layer 35, for example of AlCu, are deposited in sequence on top of the chalcogenic layer 25 33; the stack formed by the metal layer 35, the barrier

layer 34 and the chalcogenic layer 33 is defined using a same mask, thus forming a bit line 41 including a chalcogenic region 33a and metal regions 34a, 35a. Finally, a third dielectric layer 42 is deposited,
5 which is opened above the base contacts 19b. The openings thus formed are filled with tungsten to form top contacts 43 in order to prolong upwards the base contacts 19b. Then standard steps are performed for forming connection lines in contact with the top
10 contacts 43 and with the bits lines 41, pads are formed and a passivation layer 45 is deposited, defining a device main surface 46. Thus, the final structure of Figure 16 is obtained.

In practice, the strip-shaped portion 27a
15 (corresponding to the horizontal portion 102 of the first electrode 100 of Figure 4) has a longitudinal extension parallel to upper surface 16 of the substrate 11 and forms, with the bottom portion of the reduced area portion 33b, a contact area the height whereof is
20 defined by the thickness of the first conductive layer 27 and the width whereof is defined by the thickness of the sacrificial layer 31. The quality of the etching of trench 32 determines the orientation of the contact area with respect to the upper surface 16.

25 The advantages of the present invention are clear

from the above. In particular, it is outlined that the present contact structure has a very good technological repeatability, a lower dependence from the process variations than prior art solutions, while maintaining 5 a very small contact area, having sublithographic dimensions in both directions.

Finally, it is clear that numerous variations and modifications may be made to the contact structure and process described and illustrated herein, all falling 10 within the scope of the invention as defined in the attached claims.

In particular, it is stressed that the direction of the horizontal portion 102 and the first conductive layer 27 is defined with reference to the upper surface 15 92, 16 of the substrate, intending therewith a plane corresponding to the original upper surface of the wafer. In practice, the horizontal portion 102 and the first conductive layer 27 are perpendicular to the direction of growing of the substrate, due to the 20 deposition of the various superficial layers. If, due to deposition, thermal growing, etching and implant steps carried out on the wafer, the upper surface 16 of the finished device is no more planar, reference may be done to the lower surface 93 of the substrate or to the 25 device main surface 46.

Moreover we propose an alternative embodiment of the present invention in which the conductive layer 27 is in direct contact with the conductive layer 19a, thus avoiding the dielectric layers 20 and 23 and the
5 conductive layer 22.

CLAIMS

1. An electronic semiconductor device (90), comprising:

a body (91; 11) of semiconductor material having an
5 upper surface (92; 16);

a dielectric layer (95; 20, 42) extending on top of said body;

a contact structure (98) in said dielectric layer, said contact structure comprising a first conducting
10 region (102; 27a) and a second conducting region (103; 33a), said second conducting region being of chalcogenic material and being in electric contact with said first conducting region;

characterized in that said first conducting region
15 (102; 27a) has a strip-like shape having a longitudinal direction delimited by an end face (110) extending transversely to said upper surface (92; 16) and forming a contact area with said second conducting region (103; 33a).

20 2. A device according to claim 1, wherein said first conducting region (102; 27a) extends in a first direction (X) parallel to said upper surface (92; 16).

3. A device according to claim 1 or 2, wherein said end face (110) is perpendicular to said upper surface

(92; 16) within process tolerances.

4. A device according to any of claims 1-3, wherein said end face (110) has a generally rectangular shape having a height (S) and a width (W).

5 5. A device according to claim 4, wherein said height (S) is comprised between 5 nm and 50 nm and said width (W) is comprised between 5 nm and 50 nm.

6. A device according to any of claims 1-4, forming a PCM device (10) including a memory cell comprising a 10 selection element (13-15) and a storage element, said storage element being formed by a heater element (22a, 27a) including said first conducting region (27a) and a storage region (33a) comprising said second conducting region.

15 7. A device according to claim 6, wherein said selection element (13-15) is formed in said body (11), a lower electrode (19a) extends in said dielectric layer (20, 42) between said selection element and said first conducting region (27a) and an upper electrode 20 (35a) extends in said dielectric layer on said second conducting region (33a) and forms a bit line.

8. A device according to claim 7, wherein said second conducting region (33a) has a reduced area portion (33b) in contact with said first conducting

region (27a) and an upper enlarged portion extending on top of said reduced area portion and in contact with said upper electrode (35a).

9. A process for manufacturing an electronic
5 semiconductor device (10), comprising the steps of:

providing a body (91; 11) of semiconductor material having an upper surface (92; 16);

forming a dielectric layer (95; 20, 42) extending on top of said body; and

10 forming a contact structure (98) in said dielectric layer, said step of forming a contact structure comprising forming a first conducting region (102; 27a) and forming a second conducting region (103; 33a) of chalcogenic material in electric contact with said
15 first conducting region;

characterized in that said step of forming said first conducting region comprises forming a strip-shaped region (102; 27a) having a longitudinal direction delimited by an end face (110) extending
20 transversely to said upper surface (92; 16);

and said step of forming a second conducting region comprises forming said second conducting region (103; 33a) in contact with said first conducting region at said end face.

10. A process according to claim (9), wherein said end face (110) has a generally rectangular shape having a height (S) comprised between 5 nm and 50 nm and a width (W) comprised between 5 nm and 50 nm.

5 11. A process according to claim 9 or 10, wherein said step of forming said first conducting region (27a) comprises depositing a first conductive layer (27) on a bottom portion (20) of said dielectric layer (20, 42); forming a delimitation layer (29) on top of said first 10 conductive layer, said delimitation layer (29) having a step (30) with a vertical side wall surface (30); forming a sacrificial portion (31a) on said vertical side wall surface; removing said first delimitation layer (29); etching said first conductive layer (27a) 15 using said a sacrificial portion (31a) as a mask; and removing said sacrificial portion.

12. A process according to claim 11, wherein said step of forming a sacrificial portion (31a) comprises depositing a sacrificial layer on said first conducting 20 region and said delimitation layer (29) and anisotropically etching said sacrificial layer (31).

13. A process according to claim 11 or 12, wherein after removing said sacrificial portion (31a), an insulating layer (30) is deposited on said first

conducting region (27a) and said bottom portion (20) of said dielectric layer (20, 42); a trench (32) is formed to remove at least a portion of said bottom portion and an end portion of said first conducting
5 region, thereby defining said end face (110); and a second conductive layer (33) of said chalcogenic material is deposited, filling said trench (32) and contacting said end face (110).

14. A process according to claim 13, comprising the
10 step of forming a PCM device (10) including a memory cell comprising a selection element (13-15) and a storage element (33b), said storage element being formed by a heater element including said first conducting region and a storage region comprising said
15 second conducting region.

15. A process according to claim 14, comprising, after depositing said second conductive layer (33), depositing an electrode layer (35) and defining said electrode layer and said second conductive layer, to
20 define a bit line (41).

ABSTRACT

A contact structure 98 for a PCM device is formed by an elongated formation 102 having a longitudinal extension parallel to the upper surface 92 of the body 91 and an end face 110 extending in a vertical plane. The end phase 110 is in contact with a bottom portion of an active region 103 of chalcogenic material so that the dimensions of the contact area defined by the end face 110 are determined by the thickness S of the elongated formation and by the width W thereof.

Figure 4

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